

MS-7233

Version 0A
08/09/2005 Update

CPU:

Intel LGA775 Processor

System Chipset:

SIS 656 + SiS 965L

On Board Chipset:

LPC Super I/O -- W83697HF
LAN PHY -- VT6103
IEEE1394 -- VT6307
AC97 CODEC -- RealTek ALC850

CLOCK Chip :

ICS953401+ Buffer ICS9P932

Main Memory:

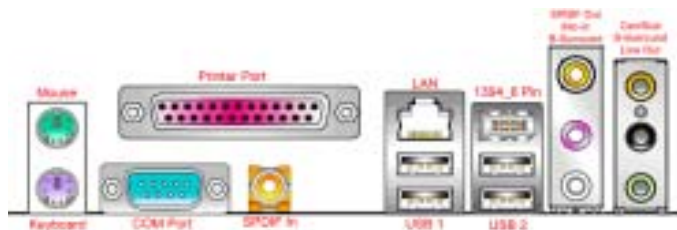
DDR2 DIMM Slot *4

Expansion Slots:

PCI EXPRESS x16 Slot *1
PCI EXPRESS x1 Slot *1
PCI2.2 Slot *2

PWM:

INTERSIL ISL6565ACV



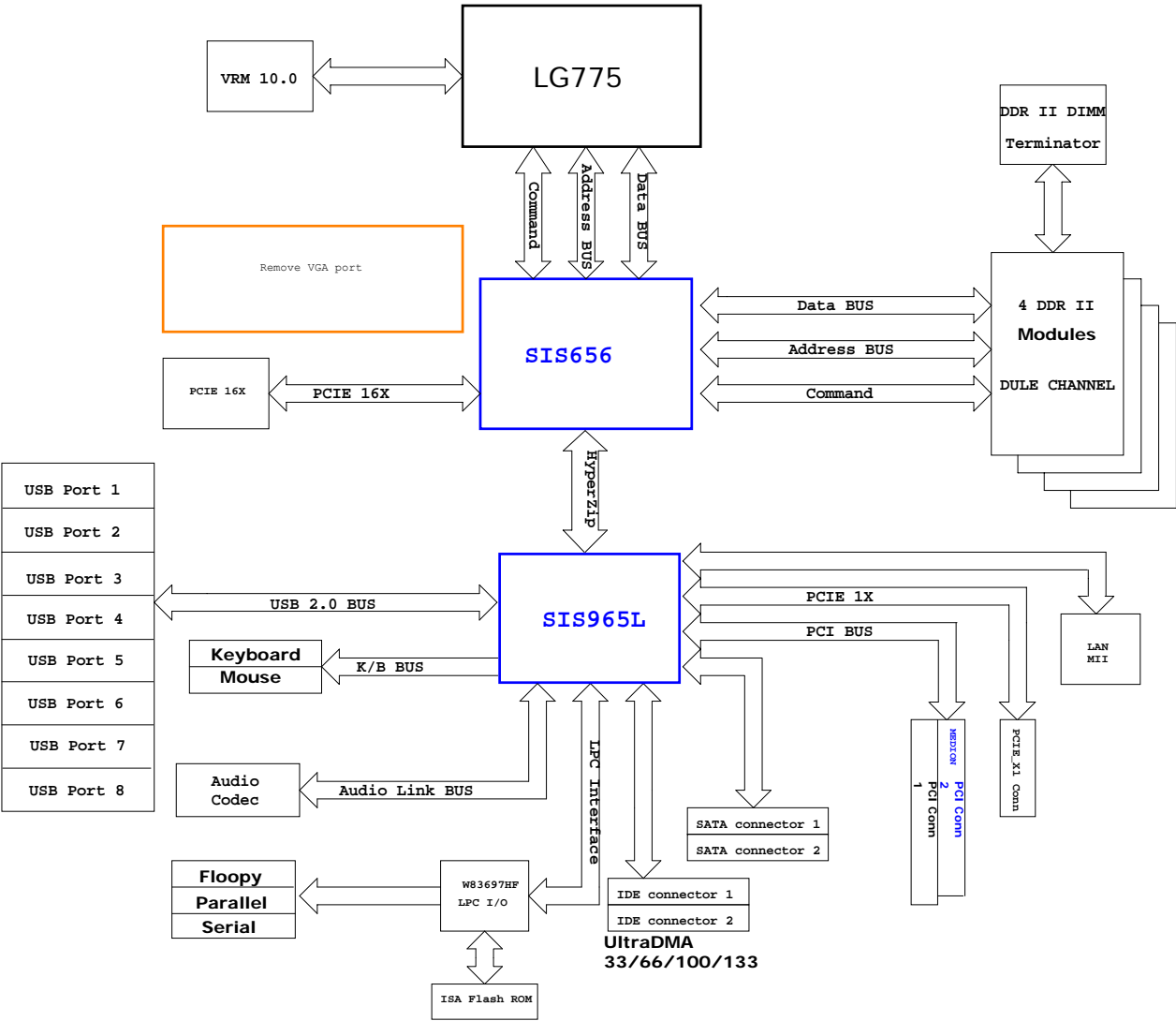
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PCI Routing

PCI 2	INTC# IDSEL=AD23 MASTER=PREQ#1 PGNT#1 PCICLK4 INTB# IDSEL=AD21 MASTER=PREQ#3 PGNT#3 PCICLK3 INTA# IDSEL=AD20 MASTER=PREQ#5 PGNT#5 PCICLK0
PCI 3	INTD# IDSEL=AD19 MASTER=PREQ#2 PGNT#2 PCICLK2
1394	INTC# IDSEL=AD22 MASTER=PREQ#4 PGNT#4 1394PCLK

Block Diagram

MS-7233 Ver:1.0

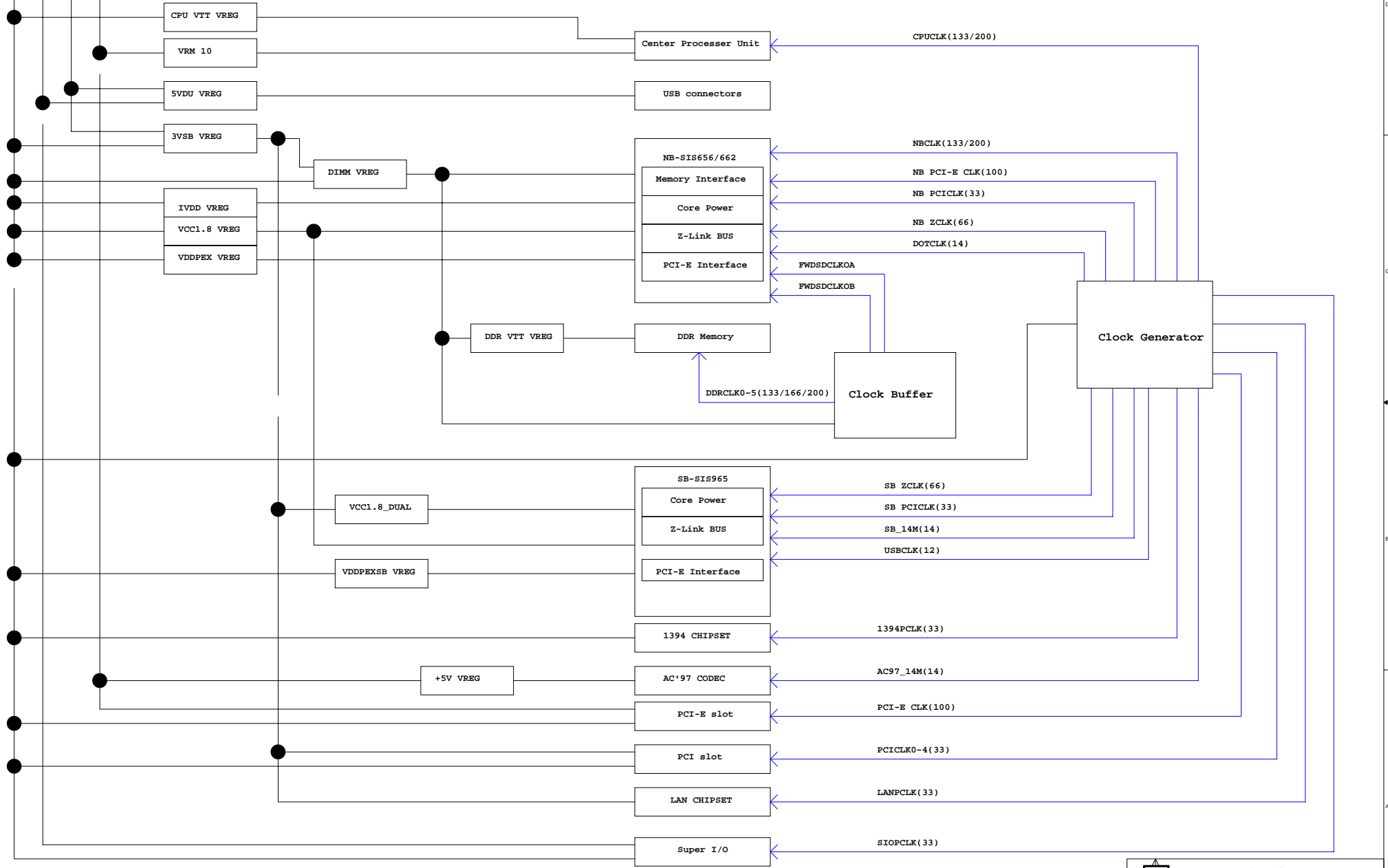


Power Delivery Map

CLOCK Delivery Map

ATX 12V POWER Supply

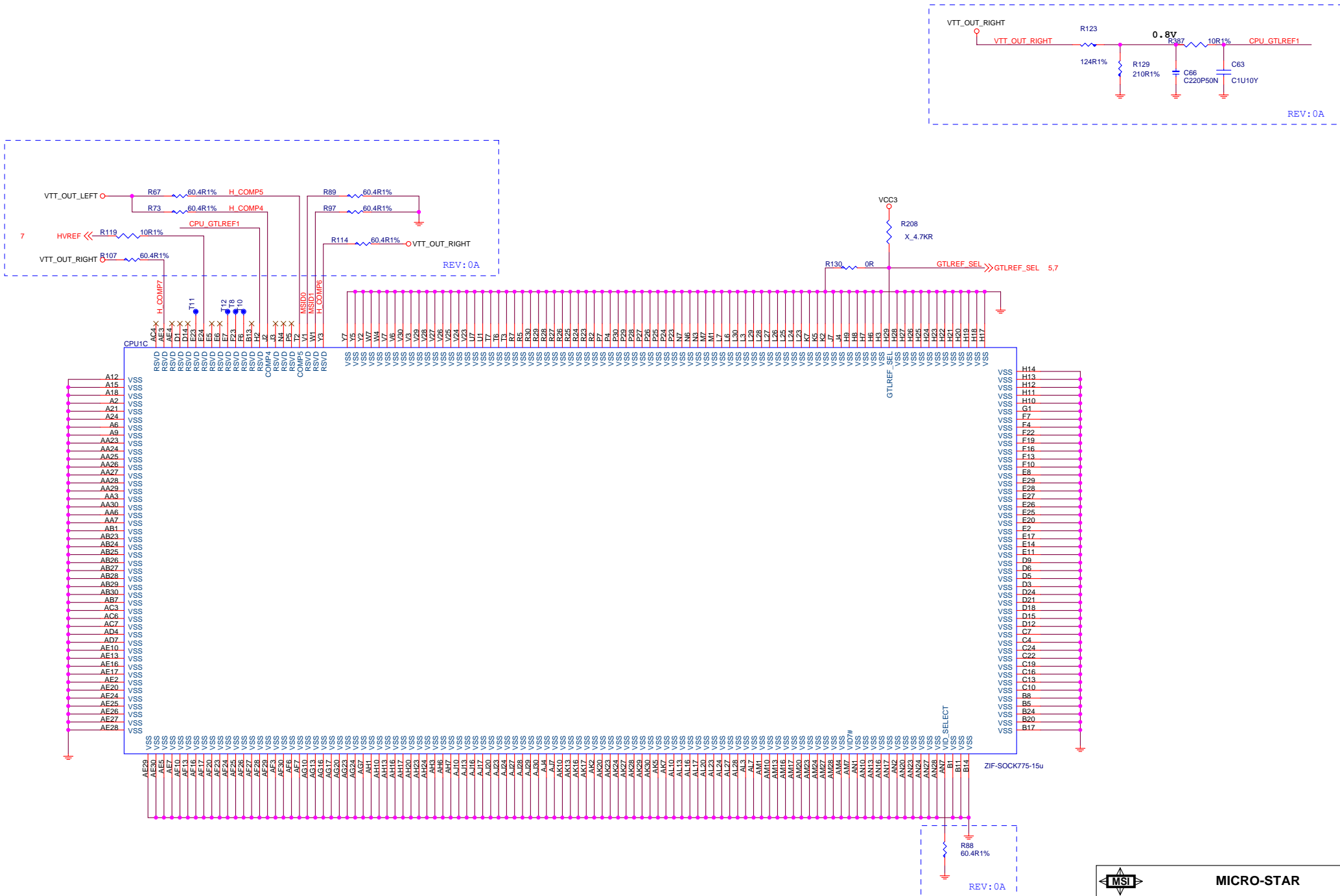
3.3V	5V	5VSB 1A	12V
------	----	------------	-----



REV: 0A



Title			
Intel LGA775 CPU - Signals			
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656-1 (Host/PCI_Express)

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MDA[0..63] << MDA[0..63] 12
DQMA[0..7] << DQMA[0..7] 12
DQSA[0..7] << DQSA[0..7] 12
DQSA#[0..7] << DQSA#[0..7] 12
MAA[0..17] << MAA[0..17] 12,14
CSA[0..3] << CSA[0..3] 12,14
ODTA[0..3] << ODTA[0..3] 12,14

MDA0 M34 MD0A
MDA1 N36 MD1A
MDA2 R36 MD2A
MDA3 R33 MD3A
MDA4 M36 MD4A
MDA5 M35 MD5A
MDA6 P34 MD6A
MDA7 P34 MD7A
DQMA0 N33 DQM0A
DQSA0 P36 DQS0A
DQSA#0 N32 DQS0A#

MDA8 T39 MD8A
MDA9 T34 MD9A
MDA10 V34 MD10A
MDA11 W36 MD11A
MDA12 R32 MD12A
MDA13 T36 MD13A
MDA14 V36 MD14A
MDA15 V36 MD15A
DQMA1 U36 DQM1A
DQSA1 U32 DQS1A
DQSA#1 U33 DQS1A#

MDA16 Y36 MD16A
MDA17 Y36 MD17A
MDA18 AB35 MD18A
MDA19 AB34 MD19A
MDA20 W33 MD20A
MDA21 W32 MD21A
MDA22 AA32 MD22A
MDA23 AB36 MD23A
DQMA2 V34 DQM2A
DQSA2 AA33 DQS2A
DQSA#2 AA36 DQS2A#

MDA24 AH30 MD24A
MDA25 AJ32 MD25A
MDA26 AM30 MD26A
MDA27 AM30 MD27A
MDA28 AC39 MD28A
MDA29 AH32 MD29A
MDA30 AM32 MD30A
MDA31 AN32 MD31A
DQMA3 AJ30 DQM3A
DQSA3 AL32 DQS3A
DQSA#3 AK32 DQS3A#

MDA32 AH24 MD32A
MDA33 AH23 MD33A
MDA34 AH21 MD34A
MDA35 AM20 MD35A
MDA36 AJ24 MD36A
MDA37 AJ23 MD37A
MDA38 AJ21 MD38A
MDA39 AH22 MD39A
DQMA4 AM22 DQM4A
DQSA4 AJ22 DQS4A
DQSA#4 AK22 DQS4A#

MDA40 AM19 MD40A
MDA41 AT18 MD41A
MDA42 AT16 MD42A
MDA43 AR16 MD43A
MDA44 AT19 MD44A
MDA45 AN19 MD45A
MDA46 AN17 MD46A
MDA47 AM17 MD47A
DQMA5 AR18 DQM5A
DQSA5 AT17 DQS5A
DQSA#5 AP18 DQS5A#

MDA48 AN15 MD48A
MDA49 AM15 MD49A
MDA50 AM13 MD50A
MDA51 AT12 MD51A
MDA52 AP16 MD52A
MDA53 AT15 MD53A
MDA54 AN13 MD54A
MDA55 AN13 MD55A
DQMA6 AT14 DQM6A
DQSA6 AP14 DQS6A
DQSA#6 AR14 DQS6A#

MDA56 AT11 MD56A
MDA57 AT11 MD57A
MDA58 AR9 MD58A
MDA59 AP9 MD59A
MDA60 AR12 MD60A
MDA61 AP12 MD61A
MDA62 AP10 MD62A
MDA63 AT9 MD63A
DQMA7 AM11 DQM7A
DQSA7 AR10 DQS7A
DQSA#7 AT10 DQS7A#

MA0A AP33 MAA0
MA1A AN33 MAA1
MA2A AT34 MAA2
MA3A AR34 MAA3
MA4A AR35 MAA4
MA5A AP34 MAA5
MA6A AP35 MAA6
MA7A AP36 MAA7
MA8A AN36 MAA8
MA9A AT33 MAA10
MA10A AR32 MAA11
MA11A AP32 MAA12
MA12A AM35 MAA13
MA13A AN34 MAA14
MA14A AM34 MAA15
MA15A AM29 MAA16
MA16A AM36 MAA17
MA17A

RASA# AT32 RASA- << RASA- 12,14
CASA# AP30 CASA- << CASA- 12,14
WEA# AT31 WEA- << WEA- 12,14

FWSDCLKOB K36 R FWSDCLKOB R333 22R FWSDCLKOB 25
FWSDCLKOB K35 R FWSDCLKOB R334 22R FWSDCLKOB 25
FWSDCLKOA K34 R FWSDCLKOA R332 22R FWSDCLKOA 25
FWSDCLKOA L36 R FWSDCLKOA R335 22R FWSDCLKOA 25

CS0A# AM31 CSA-0
CS1A# AN29 CSA-1
CS2A# AN31 CSA-2
CS3A# AT29 CSA-3
ODT0A AR30 ODTA0
ODT1A AP28 ODTA1
ODT2A AT30 ODTA2
ODT3A AR28 ODTA3
GCKE AJ33 X

ECCD0A/CKE0A AH34 CKEA0 << CKEA0 12,14
ECCD1A/CKE1A AJ36 CKEA1 << CKEA1 12,14
ECCD2A/CKE2A AL34 CKEA2 << CKEA2 12,14
ECCD3A/CKE3A AL33 CKEA3 << CKEA3 12,14
ECCD4A AH36
ECCD5A AK34
ECCD6A AL36
ECCD7A AJ34
ECCDQMA MD39A
ECCDQSA AK35
ECCDQSA# AK36

D1XAVDD A13 D1XAVDD
D1XAVSS B13 D1XAVSS
D4XAVDD AH28 D4XAVDD
D4XAVSS AJ28 D4XAVSS

DDRVREF0 AE19 DDRVREF
DDRVREF1 AE23
DDRVREF2 AC25
DDRVREF3 V25

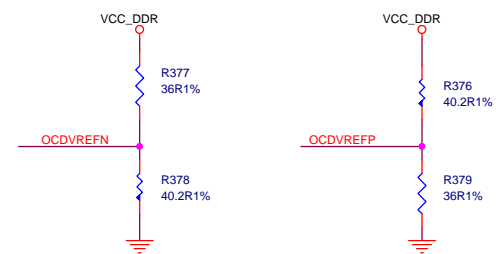
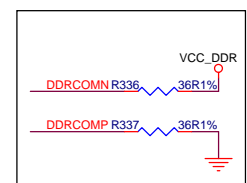
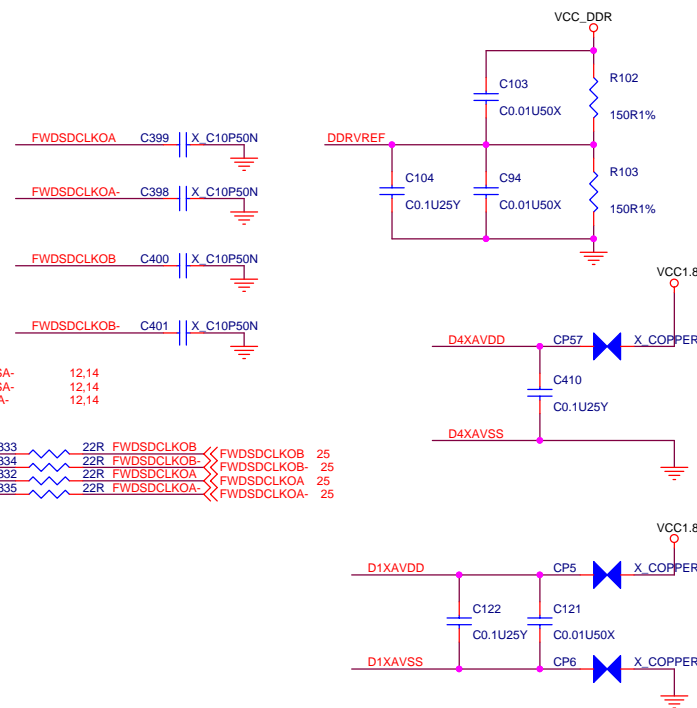
DDRCOMP AJ29 DDRCOMP
DDRCOMN AH29 DDRCOMN

OCDVREFP AR8 OCDVREFP
OCDVREFN AT8 OCDVREFN

S3AUXSW# E13 S3AUXSW# << S3AUXSW# 34

DRAM_SEL B11
SIS656

When DDR2 remove
external pull-up = DDR
R380 X_OR



MSI MICRO-STAR

Title: 656-2 (SDRAM A)

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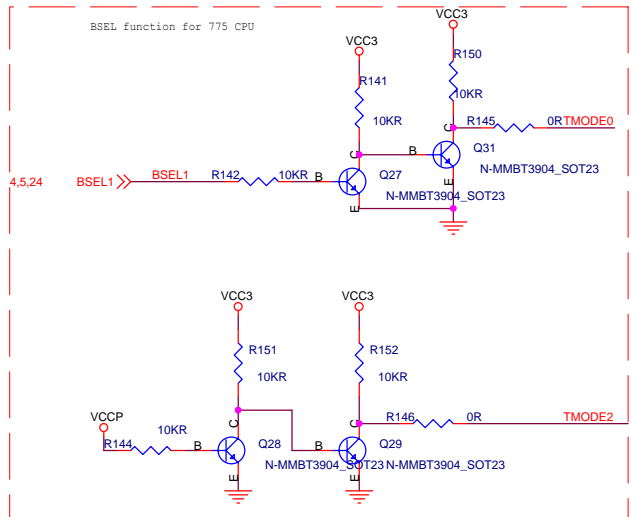
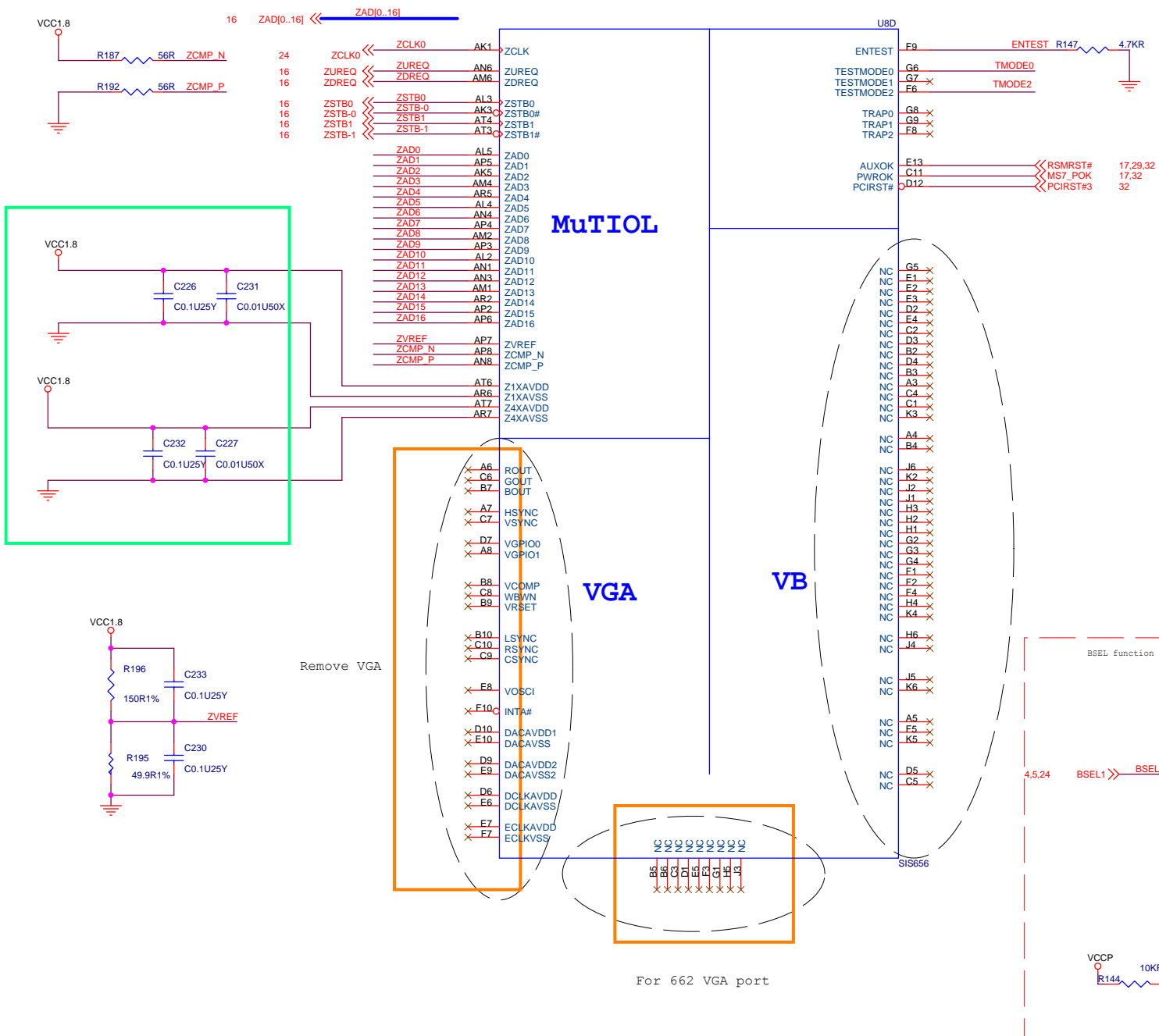
MD8[0..63] << MD8[0..63] 13
DQMB[0..7] << DQMB[0..7] 13
DQSB[0..7] << DQSB[0..7] 13
DQSB#[0..7] << DQSB#[0..7] 13
MAB[0..17] << MAB[0..17] 13,15
CSB-[0..3] << CSB-[0..3] 13,15
ODTB[0..3] << ODTB[0..3] 13,15

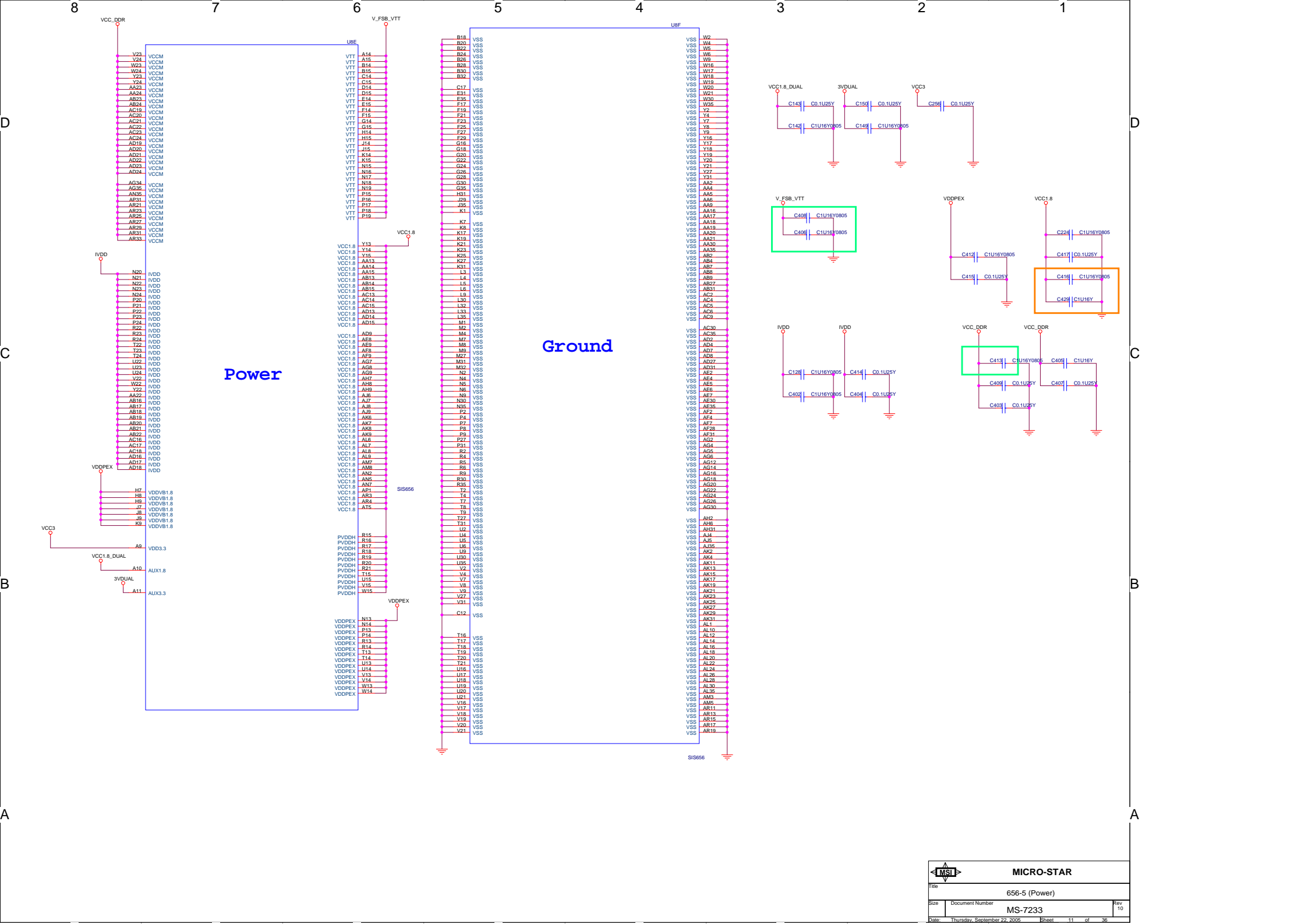
MD80 N29 MD0B
MD81 M28 MD1B
MD82 P28 MD2B
MD83 R28 MD3B
MD84 M30 MD4B
MD85 M29 MD5B
MD86 P29 MD6B
MD87 R29 MD7B
DQMB0 N28 DQMB0B
DQSB0 P30 DQS0B
DQSB#0 P32 DQS0B#
MD88 T29 MD8B
MD89 U29 MD9B
MD810 W29 MD10B
MD811 V28 MD11B
MD812 T32 MD12B
MD813 V30 MD13B
MD814 V30 MD14B
MD815 V29 MD15B
DQMB1 T28 DQM1B
DQSB1 V32 DQS1B
DQSB#1 U28 DQS1B#
MD816 Y30 MD16B
MD817 Y29 MD17B
MD818 AB29 MD18B
MD819 AC29 MD19B
MD820 W28 MD20B
MD821 Y32 MD21B
MD822 AB32 MD22B
MD823 AB30 MD23B
DQMB2 AA29 DQM2B
DQSB2 AA28 DQS2B
DQSB#2 Y28 DQS2B#
MD824 AD32 MD24B
MD825 AD30 MD25B
MD826 AE30 MD26B
MD827 AF29 MD27B
MD828 AB28 MD28B
MD829 AC28 MD29B
MD830 AE28 MD30B
MD831 AF32 MD31B
DQMB3 AD29 DQM3B
DQSB3 AD28 DQS3B
DQSB#3 AE29 DQS3B#
MD832 AJ27 MD32B
MD833 AM26 MD33B
MD834 AM24 MD34B
MD835 AK24 MD35B
MD836 AM28 MD36B
MD837 AK28 MD37B
MD838 AH26 MD38B
MD839 AH25 MD39B
DQMB4 AK26 DQM4B
DQSB4 AJ25 DQS4B
DQSB#4 AJ26 DQS4B#
MD840 AJ19 MD40B
MD841 AH20 MD41B
MD842 AH18 MD42B
MD843 AH17 MD43B
MD844 AK20 MD44B
MD845 AJ20 MD45B
MD846 AJ18 MD46B
MD847 AJ17 MD47B
DQMB5 AH19 DQM5B
DQSB5 AK18 DQS5B
DQSB#5 AM18 DQS5B#
MD848 AJ16 MD48B
MD849 AJ15 MD49B
MD850 AJ13 MD50B
MD851 AH14 MD51B
MD852 AM16 MD52B
MD853 AK16 MD53B
MD854 AK14 MD54B
MD855 AJ14 MD55B
DQMB6 AH16 DQM6B
DQSB6 AM14 DQS6B
DQSB#6 AH15 DQS6B#
MD856 AK12 MD56B
MD857 AJ12 MD57B
MD858 AN9 MD58B
MD859 AM9 MD59B
MD860 AH13 MD60B
MD861 AM12 MD61B
MD862 AM10 MD62B
MD863 AK10 MD63B
DQMB7 AJ11 DQM7B
DQSB7 AH11 DQS7B
DQSB#7 AH12 DQS7B#

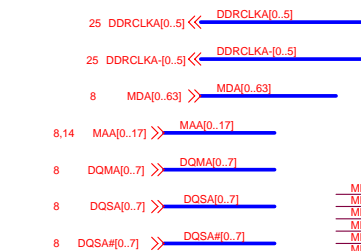
MA0B AT25 MAB0
MA1B AN25 MAB1
MA2B AM25 MAB2
MA3B AT26 MAB3
MA4B AR26 MAB4
MA5B AP26 MAB5
MA6B AT27 MAB6
MA7B AM27 MAB7
MA8B AN27 MAB8
MA9B AG32 MAB9
MA10B AP24 MAB10
MA11B AT24 MAB11
MA12B AR24 MAB12
MA13B AG36 MAB13
MA14B AT28 MAB14
MA15B AG33 MAB15
MA16B AN21 MAB16
MA17B AF34 MAB17
RASB# AT23 RASB- << RASB- 13,15
CASB# AR22 CASB- << CASB- 13,15
WEB# AT22 WEB- << WEB- 13,15
ECCD0B/CKE0B AC32 CKEB0 << CKEB0 13,15
ECCD1B/CKE1B AD36 CKEB1 << CKEB1 13,15
ECCD2B/CKE2B AF36 CKEB2 << CKEB2 13,15
ECCD3B/CKE3B AF35 CKEB3 << CKEB3 13,15
ECCD4B AC36 << <<
ECCD5B AC33 << <<
ECCD6B AE32 << <<
ECCD7B AD35 << <<
ECCD0MB AE36 << <<
ECCDQSB# AD34 << <<
CS0B# AN23 CSB-0
CS1B# AM21 CSB-1
CS2B# AM23 CSB-2
CS3B# AT20 CSB-3
ODT0B AP22 ODTB0
ODT1B AR20 ODTB1
ODT2B AT21 ODTB2
ODT3B AP20 ODTB3

U8C

SIS656







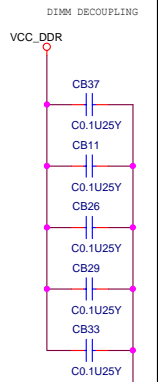
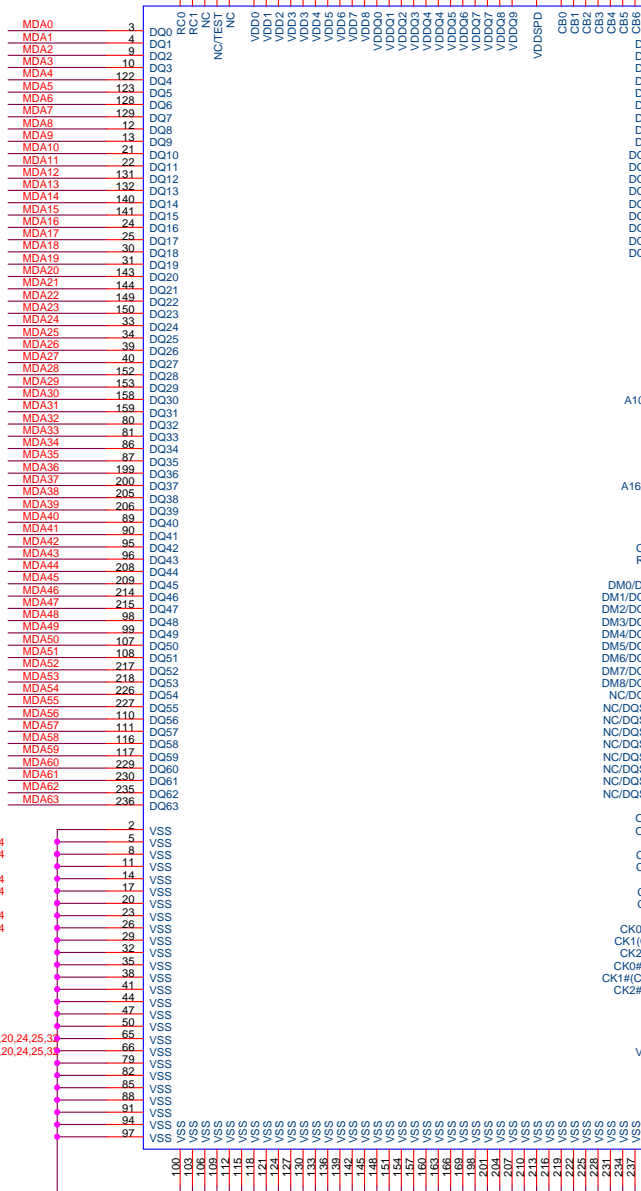
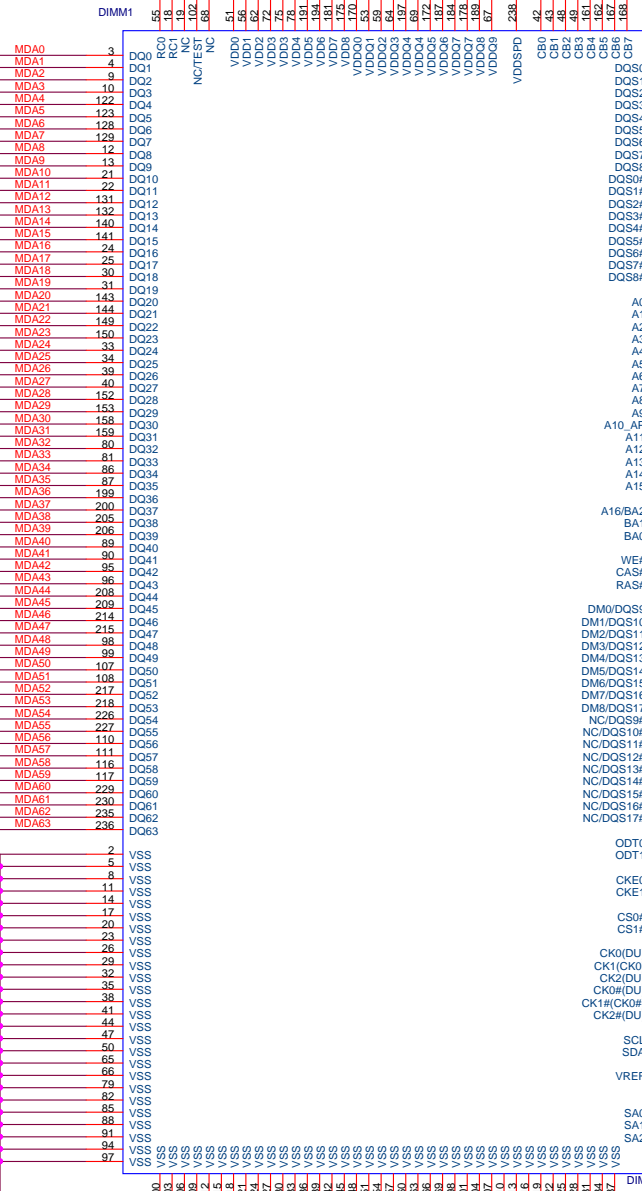
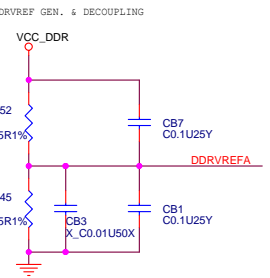
NOTE:

VDDID IS A TRAP ON THE DIMM MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7



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25 DDRCLKB[0..5] << DDRCLKB[0..5]
25 DDRCLKB[0..5] << DDRCLKB[0..5]

9 MDB[0..63] >> MDB[0..63]
9,15 MAB[0..17] >> MAB[0..17]
9 DQMB[0..7] >> DQMB[0..7]
9 DQSB[0..7] >> DQSB[0..7]
9 DQSB#0..7 >> DQSB#0..7

NOTE:

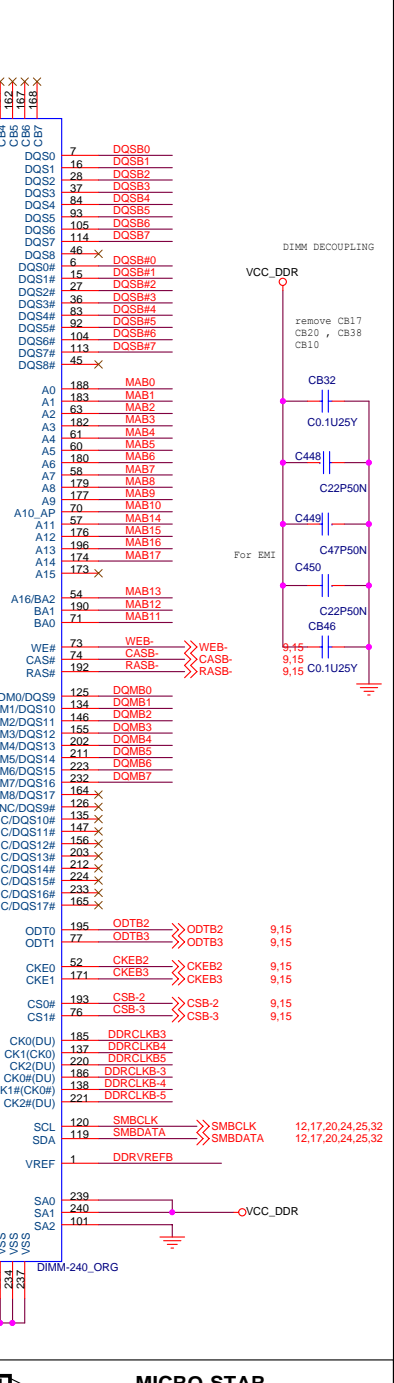
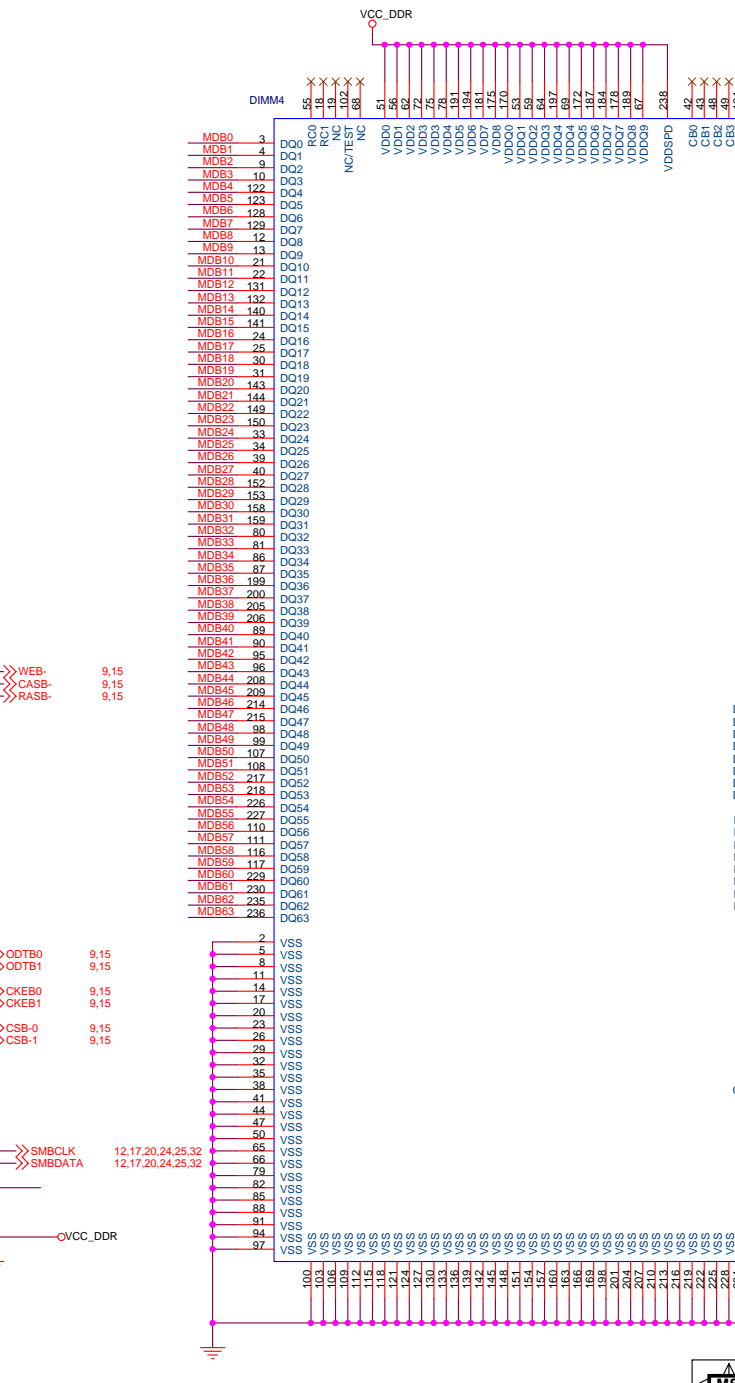
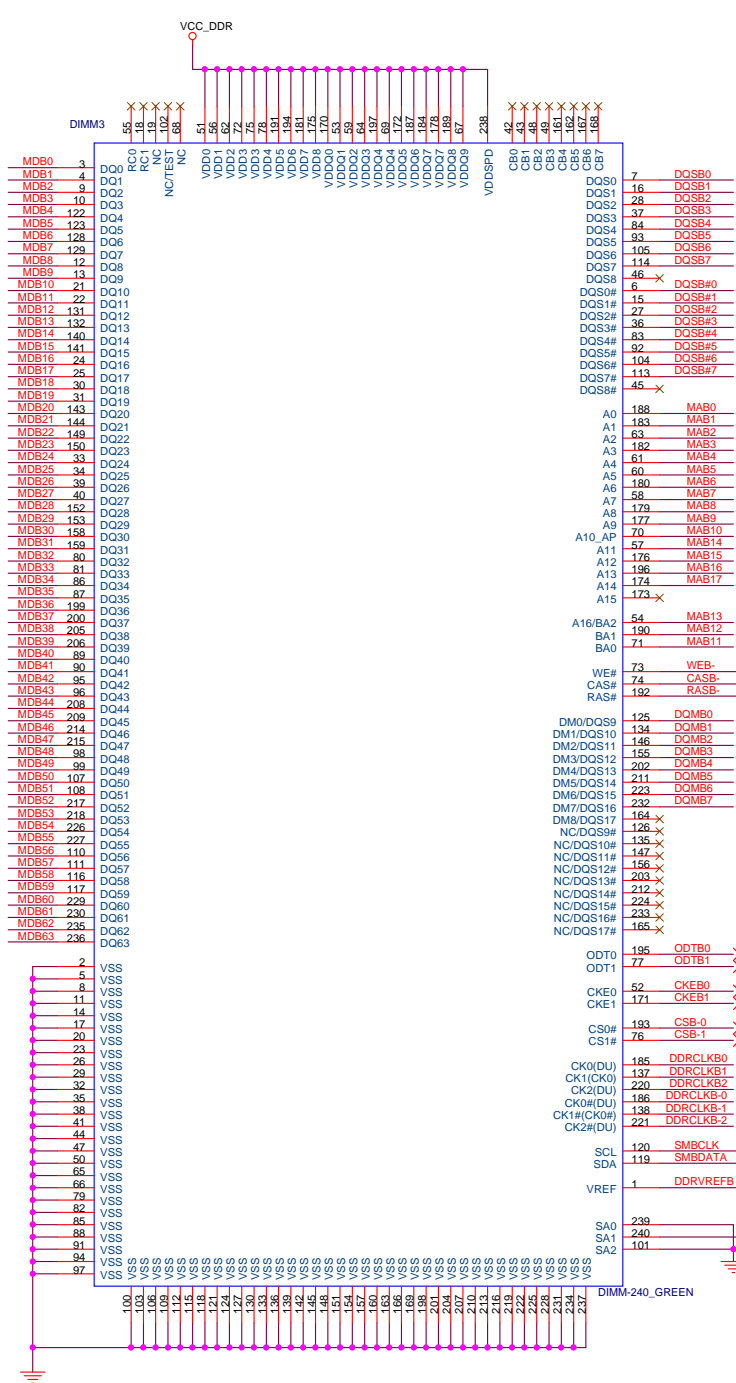
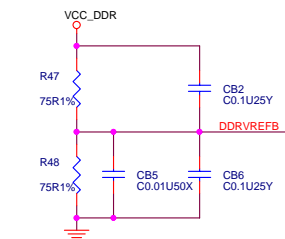
VDDID IS A TRAP ON THE DIMM
MODULE TO INDICATE:

VDDID	REQUIRED POWER
OPEN	VDD=VDDQ
GND	VDDI=VDDQ

MEMORY MUX TABLE:

SDR	DDR
CS0	CS0
CS1	CS1
CS2	CS2
CS3	CS3
CS4	CS4
CS5	CS5
CSB0	DQS0
CSB1	DQS1
CSB2	DQS2
CSB3	DQS3
CSB4	DQS4
CSB5	DQS5
CSB6	DQS6
CSB7	DQS7

DDRREF GEN. & DECOUPLING

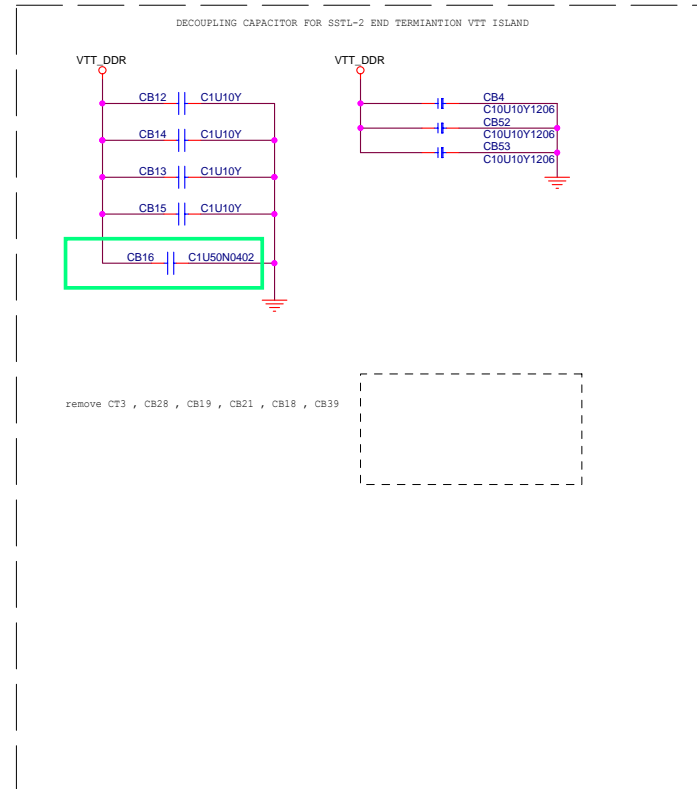
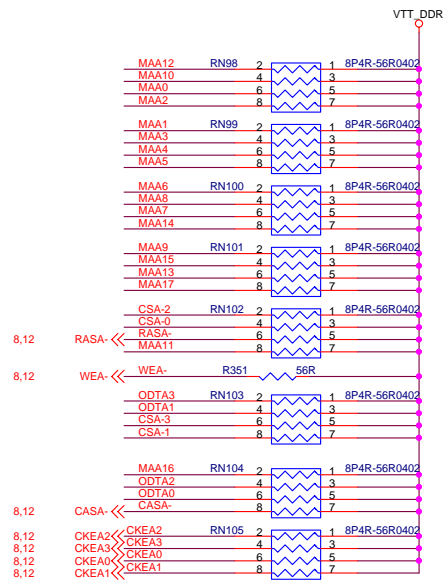


DDR TERMINATOR

SSTL-2 Termination Resistors

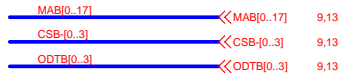


	SDR			DDR			
MD/DQM (/DQS)	LV-CMOS		0/10/-	SSTL-2		0	03
MA/Control	LV-CMOS		0	SSTL-2		0	03
CS	LV-CMOS		0	SSTL-2		0	47
WE	0D 3.3V			0D 2.5V			

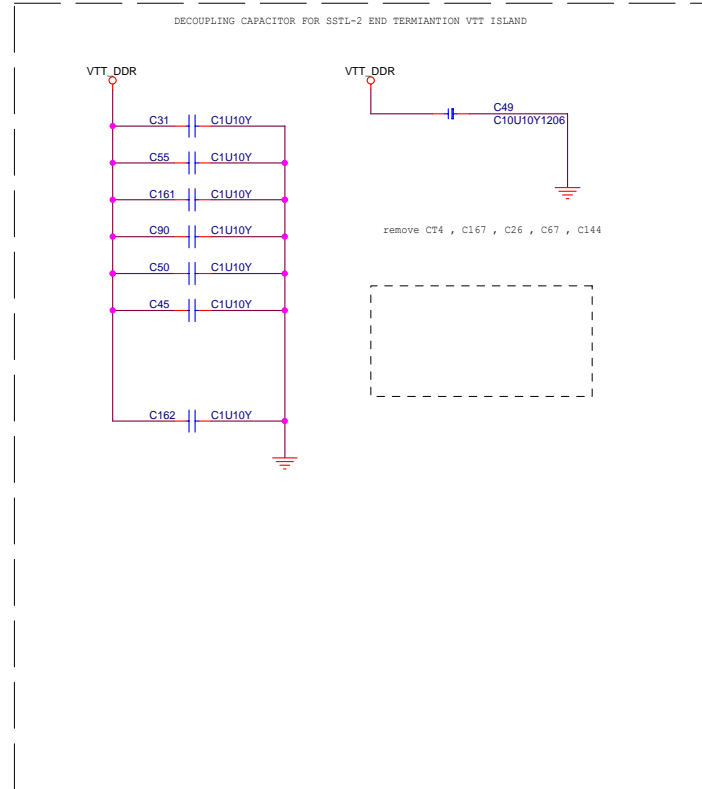
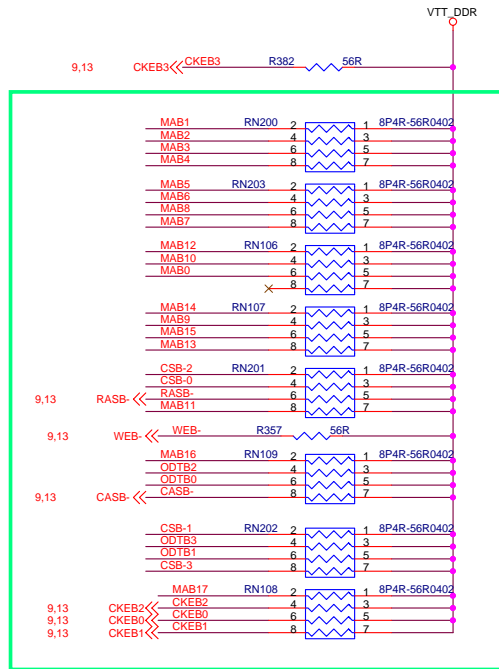


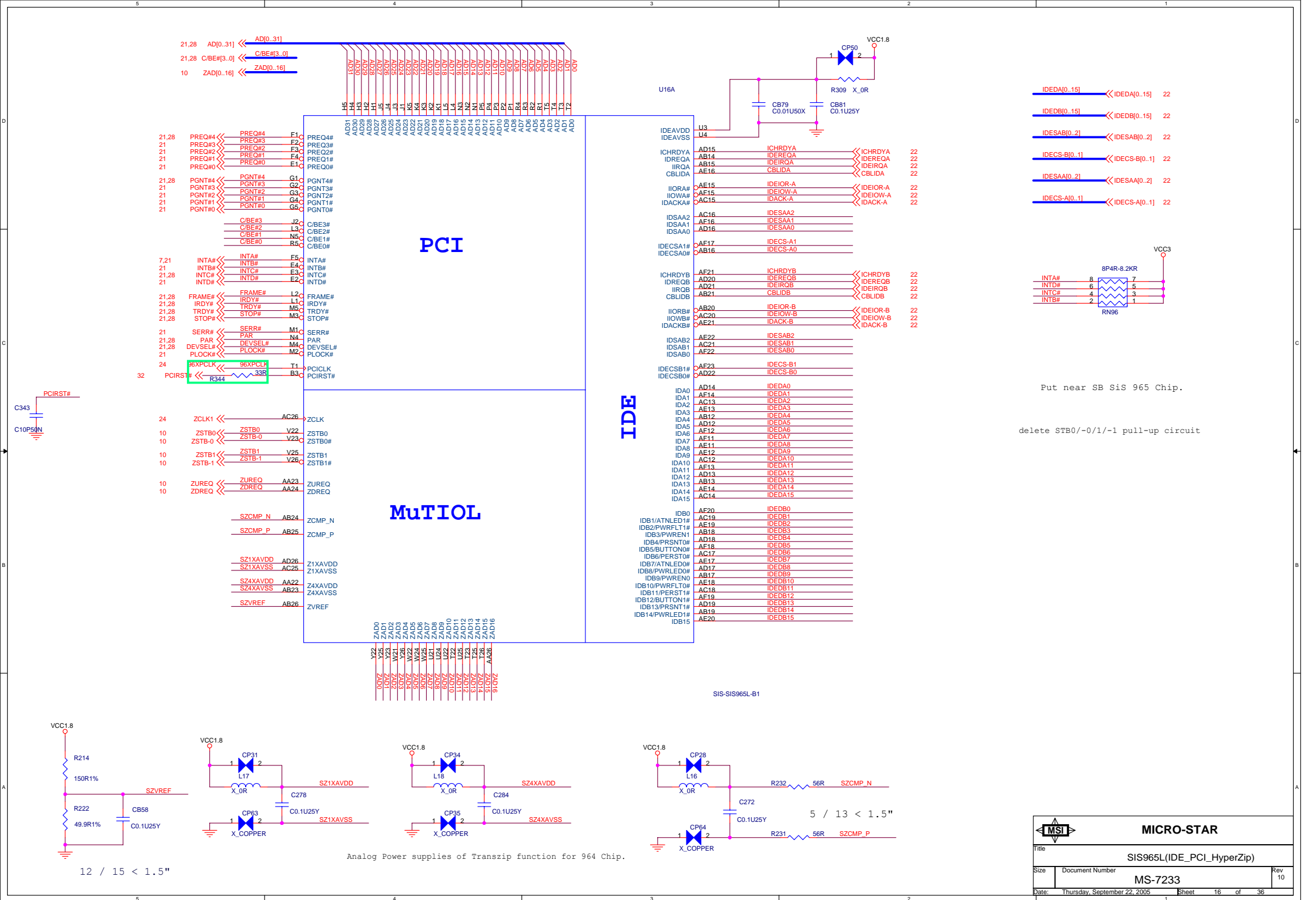
DDR TERMINATOR

SSTL-2 Termination Resistors



	DDR		DDR		
AD/DQM (/DQS)	LV-CMOS	R _s	SSTL-2	R _s	RTT
BA/Control	LV-CMOS	0/10/-	SSTL-2	10	33
CS	LV-CMOS	10	SSTL-2	0	33
CKE	0d 3.3V	0	SSTL-2	0d 2.5V	47





4 HINIT# AC23
4 A20M# AE26
4 SMI# AD23
4 INTR AC22
4 NMI AE25
4.5 IGNNE# AF25
4.5 FERR# AE24
4 STPCLK# AF24
4 SLP# AD24

VCC3 R220 10KR AF24
4.5 PROCHOT# AD25
4.5 THERMTRIP# AC24

27 LAD0 Y5
27 LAD1 Y4
27 LAD2 AA2
27 LAD3 AA3
27 LFRAME# AA1
27 LDRQ# AA4
27 LDRQ# SIRO# AA5

12,13,20,24,25,32 SMBDATA W5
12,13,20,24,25,32 SMBCLK W4

26 AC_SDIN0 E6
26 AC_SDIN1 B4
26 AC_SDOUT W3
26 AC_SYNC W2
26 AC_RST# B5
26 AC_BITCLK W1

24 SB14M Y2
34 SPK D1
34 PWRBTN# D5
20,21,27,28 PME# A6
34 PSN# E7

10,29,32 RSMRST# X
GPIO13 B2
GPIO14 A5

30 KBDAT C7
30 KBCLK B7
30 MSDAT D7
30 MSCLK D6

CPU_S

APIC

LPC

RTC

SMBUS

AC'97

ACPI/Others

KBC
Keyboard
/Mouse

GMII/RGMII

PCI
Express

GPIO

U16B

TXCLK B8
GTCLK A10
EXTCLK A13

TXEN B10
TXER D11

TXD0 C8
TXD1 C9
TXD2 A9
TXD3 E9
TXD4 D8
TXD5 E10
TXD6 D8
TXD7 C10

RGMCMCP N
RGMCMCP P
RGMVREF

RXCCLK A11
RXDV E11
RXER E11

RXD0 C13
RXD1 C12
RXD2 A12
RXD3 B12
RXD4 D13
RXD5 E14
RXD6 E13
RXD7 E12

COL F11
CRS F12
MDC F13
MDIO F14

PRX0+ M26
PRX0- M25
PTX0+ N24
PTX0- N23
PRX1+ K26
PRX1- K25
PTX1+ L24
PTX1- L23

NC11 F26
NC10 F25
NC9 G24
NC8 G23
NC7 H26
NC6 H25
NC5 J24
NC4 J23

PCLK100P P26
PCLK100N P25
PEXTRXAVDD P25
PEXTRXAVSS P25
RSET0 P22
RSET1 P21

GPIO0/SPDIF U5
GPIO1/LDRQ1# AA6
GPIO2/THERM# V5
GPIO3/EXTSMI# V4
GPIO4/CLKRUN# V3
GPIO5/PREQ5# V2
GPIO6/PGNT5# V1
GPIO7 GPIO8
GPIO8/RING C6
GPIO9/AC_SDIN2 C4
GPIO10/AC_SDIN3 C5
GPIO11/OSC25M/STP_PC# E6
GPIO12/CPUSTP# E5

SIS-SIS965L-B1

20040319
SiS garychen [garychen@sis.com] suggestion :
I think Pull-up resistors in LADs, LDREQ, and SRQ, are not necessary. However, I still recommend you to have these pads reserved in case of any problems in the future.

GPI5 GPO5	APC1[2] = 0 , APC168[5] = 1 APC1[2] = 0 , APC168[5] = 0
GPI6 GPO6	APC1[2] = 0 , APC168[6] = 1 APC1[2] = 0 , APC168[6] = 0
PREQ5# PGNT#5	APC1[2] = 1

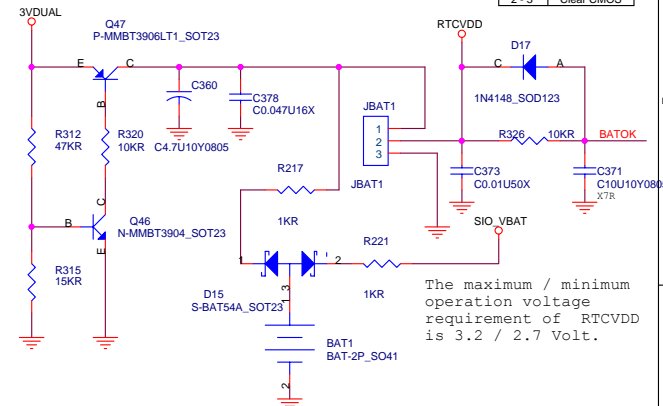
Power on --> APC1[2] = 0h
ACPI68 = Fh

RTCVDV should
be more than
30 mils width

BATTERY BLOCK

CMOS CLEAR JUMPER

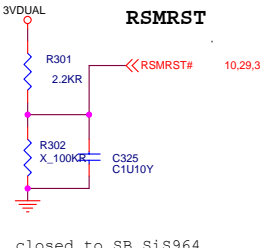
JBAT1	Clear CMOS
1-2	Normal
2-3	Clear CMOS



The maximum / minimum
operation voltage
requirement of RTCVDV
is 3.2 / 2.7 Volt.

RSMRST

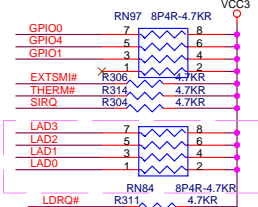
AC'97 Pull-Down



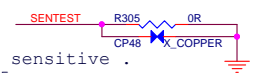
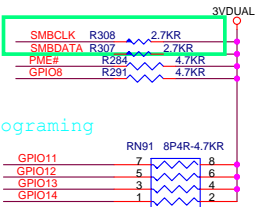
AC'97 Pull-Down:
In order to stabilize



NEED NOT
to place close to SB Sis964
GPIO 0~7 INTERNAL PULL UP
GPIO 9,10 INTERNAL PULL DOWN
Register 72 ~ 73



HW programming



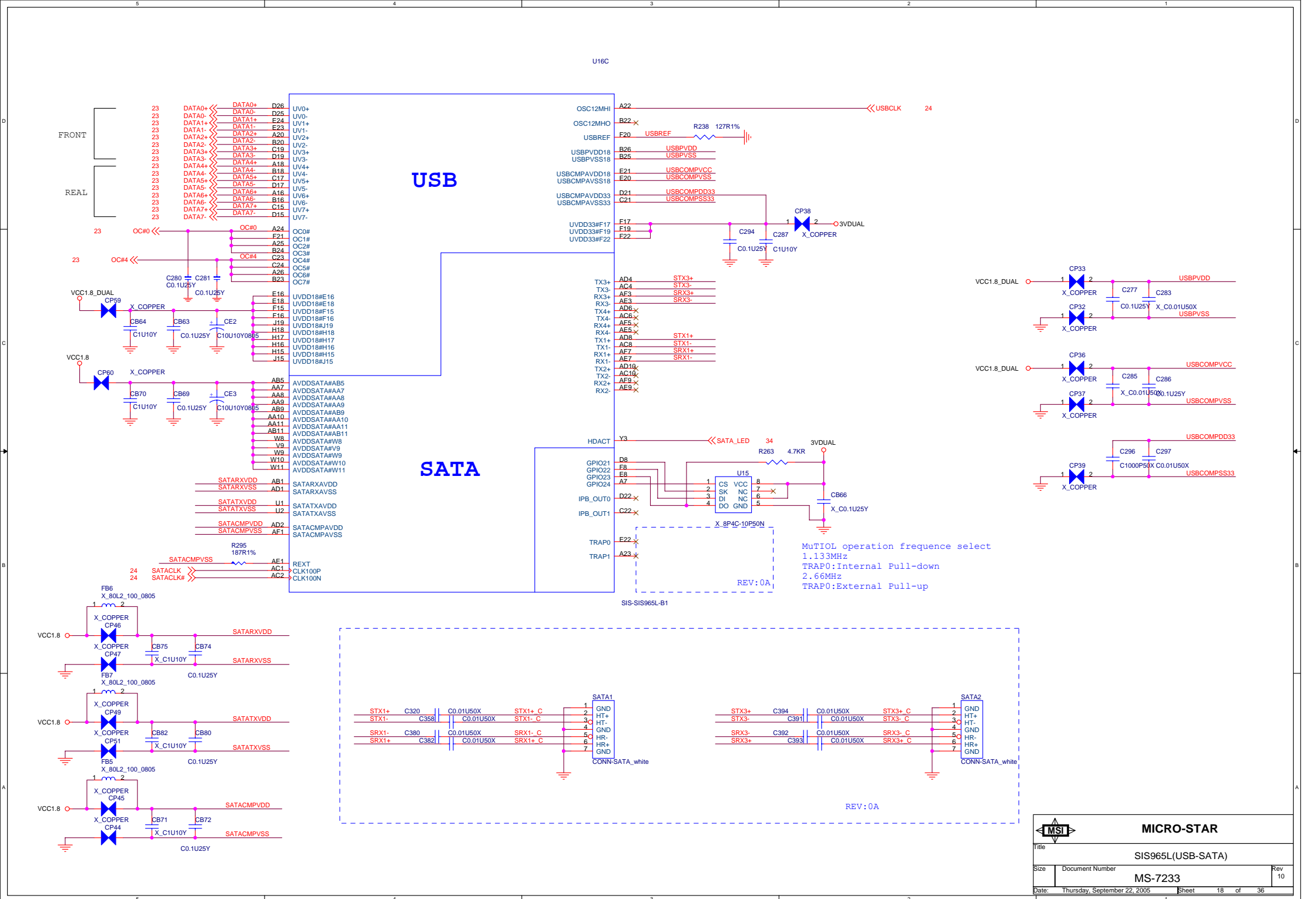
ENTEST pin is sensitive .
5 / 15

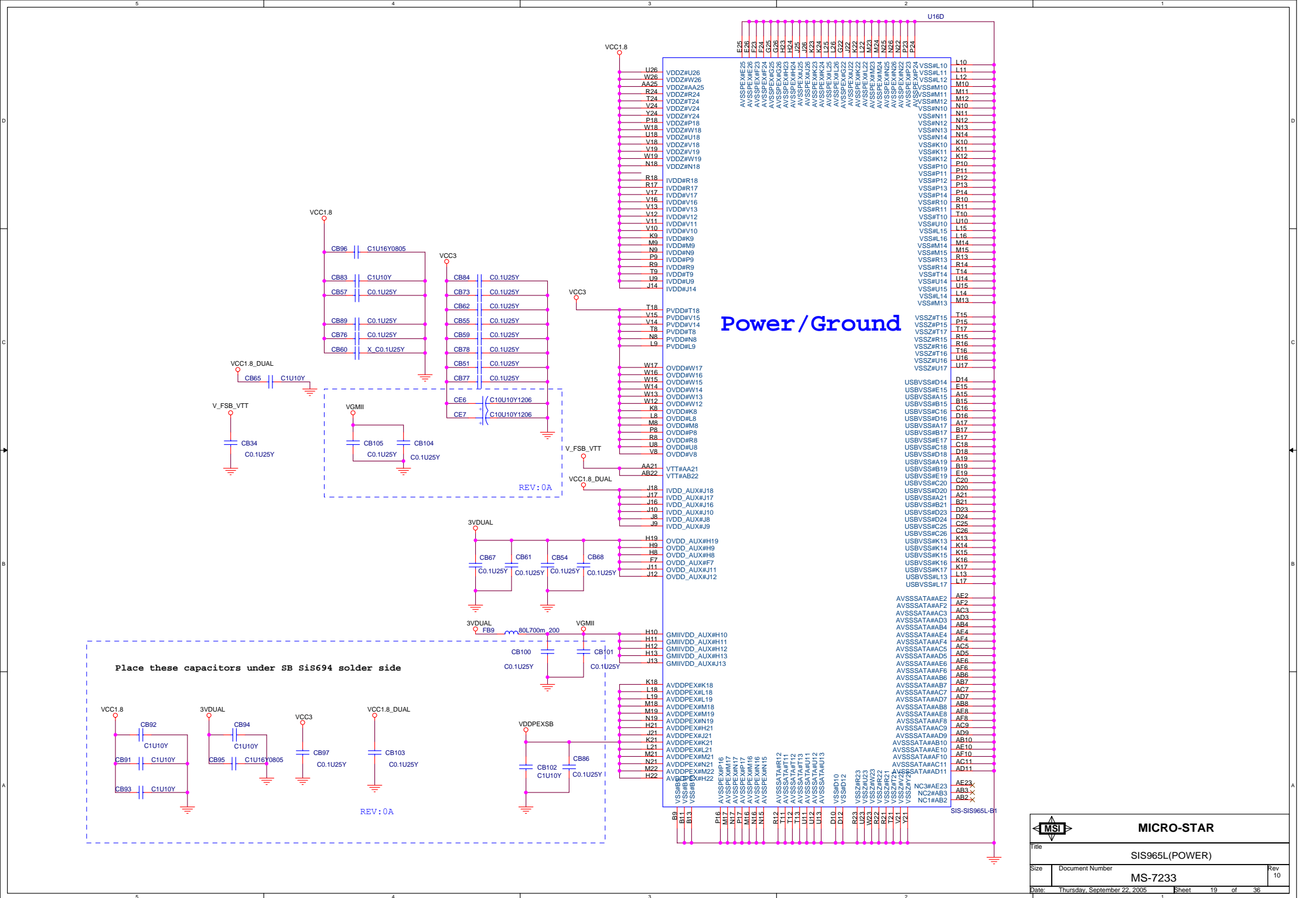
MICRO-STAR

Title: SIS965L(MISC.)

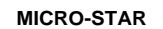
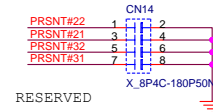
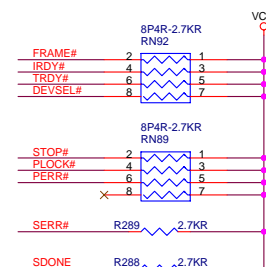
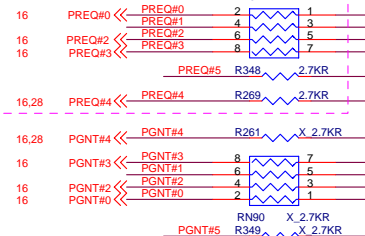
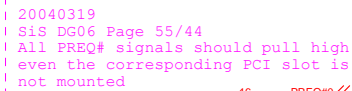
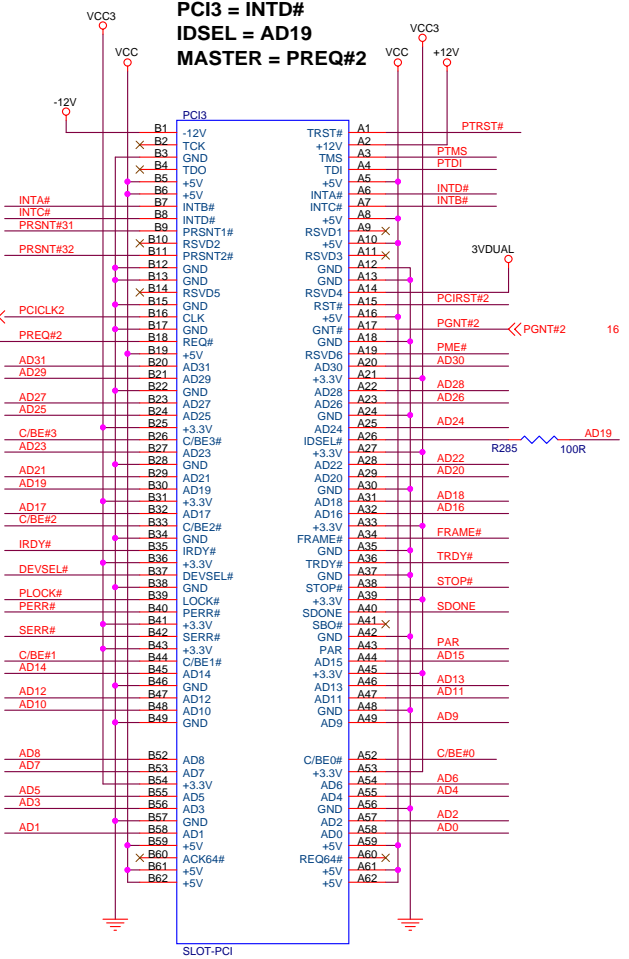
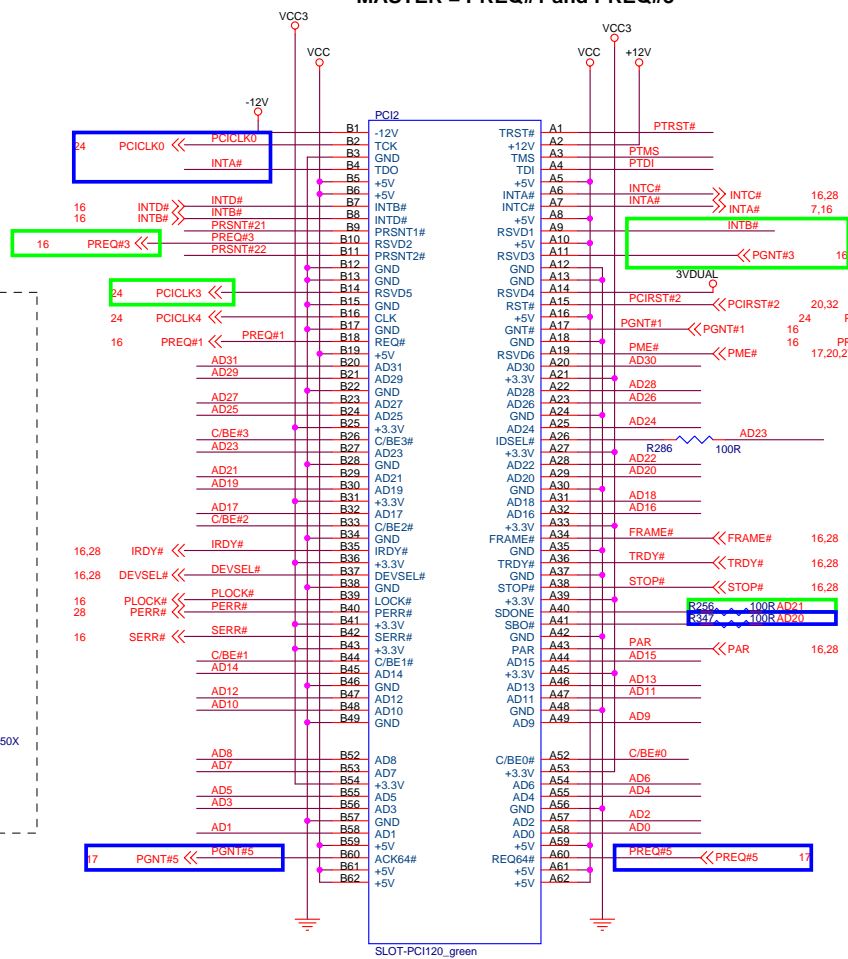
Size: Document Number: MS-7233

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PCI2 = INTC# and INTB#
IDSEL = AD23 and AD21
MASTER = PREQ#1 and PREQ#3



Title	PCI slot 1 & 2 & 3
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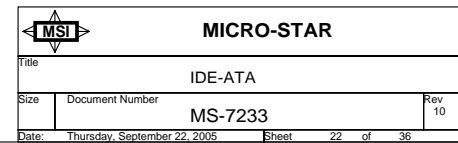
Size	Document Number
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MS-7233

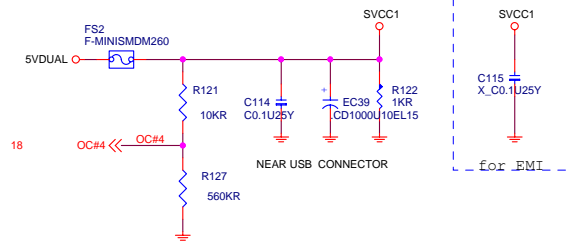
Date: Thursday, September 22, 2005 Sheet 21 of 36

Date: Thursday, September 22, 2005 Sheet 21 of 36

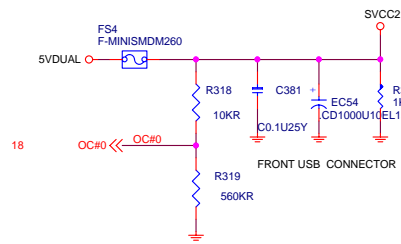
20040319
SiS AP note : A964008



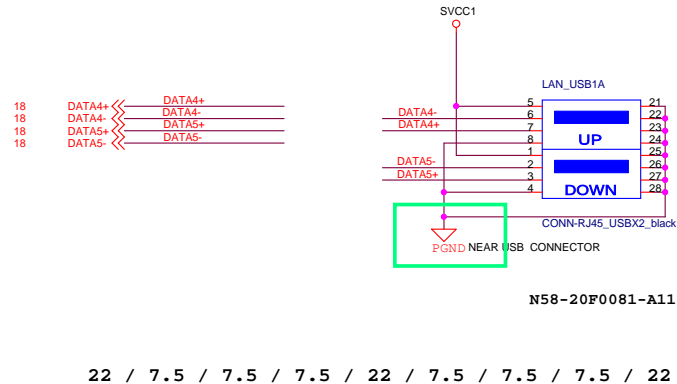
POWER CIRCUIT FOR USB PORT 4,5,6,7



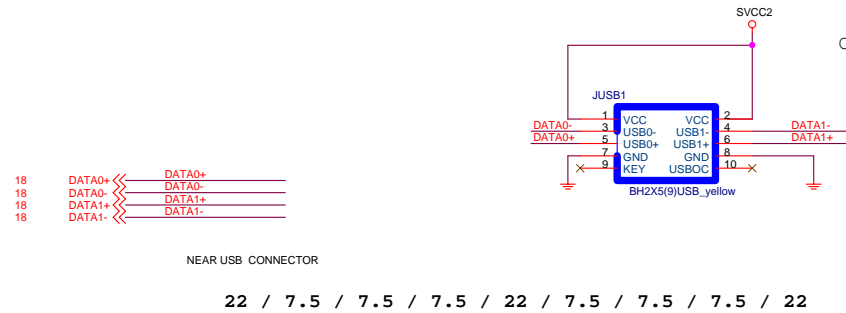
POWER CIRCUIT FOR USB PORT 0,1,2,3



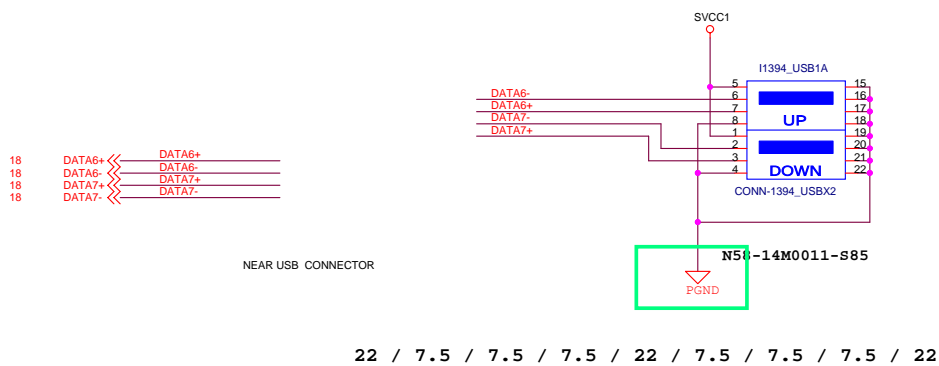
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



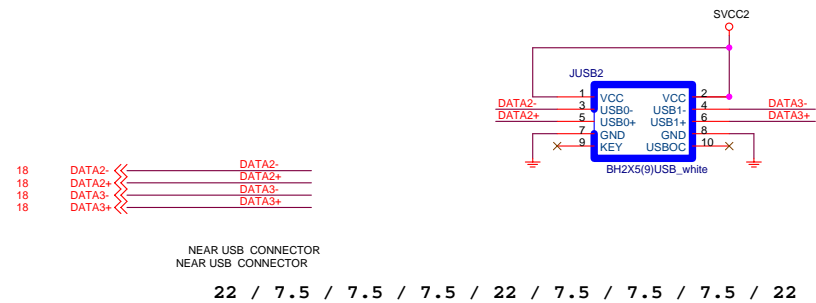
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 6,7

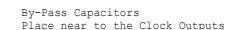


FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



OPTIONS

1. ICS953401

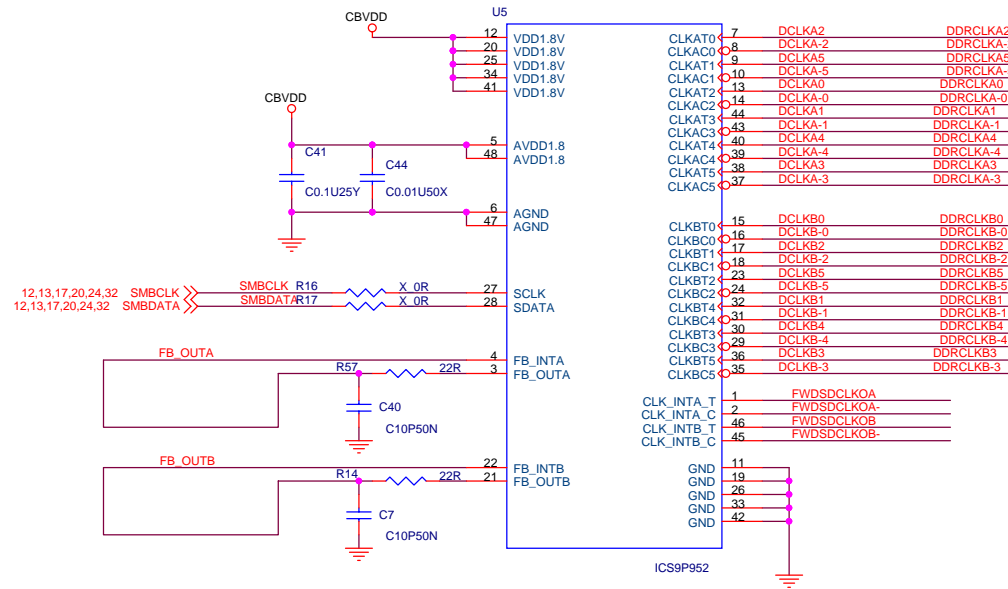
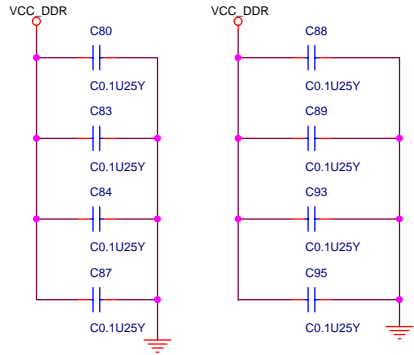


PCICLK0	PCI2 master3
PCICLK2	PCI3
PCICLK3	PCI2 master2
PCICLK4	PCI2 master1

Clock Buffer (DDR II)

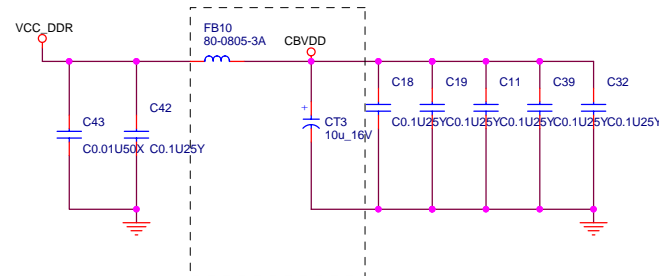
By-Pass Capacitors
Place near to the Clock Buffer

Remove demping resister



DDRVREF GEN. & DECOUPLING

change CP2 to bead



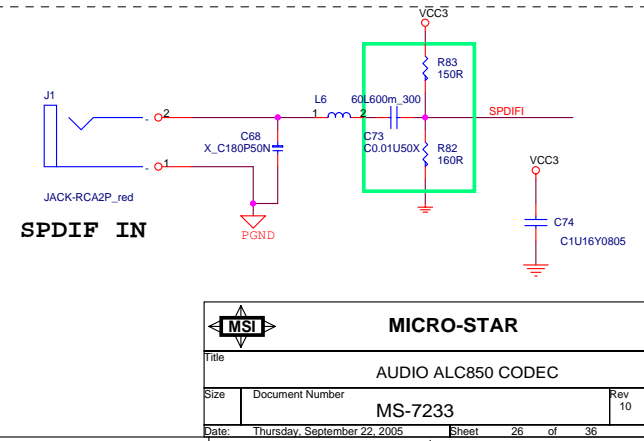
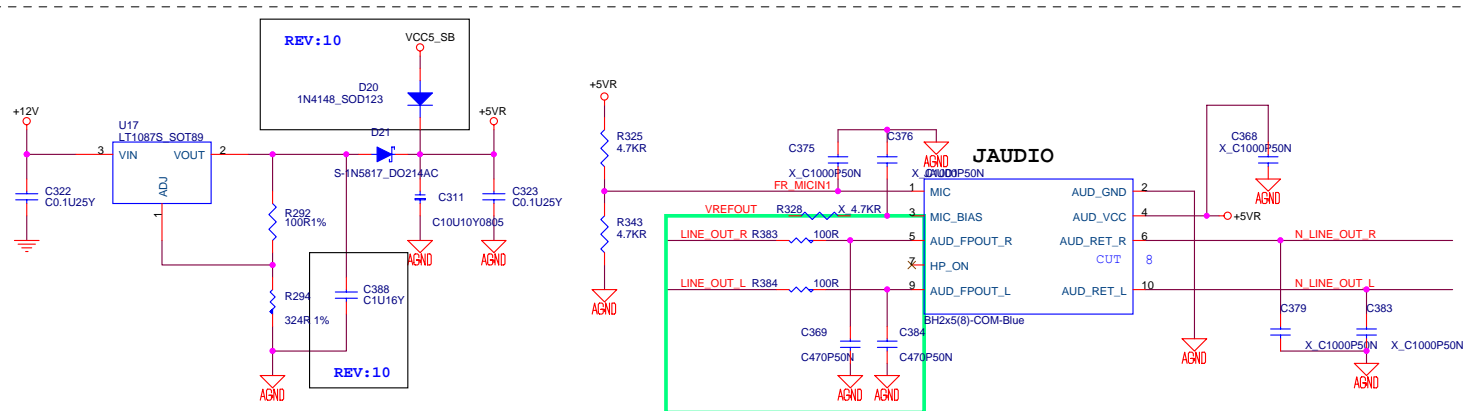
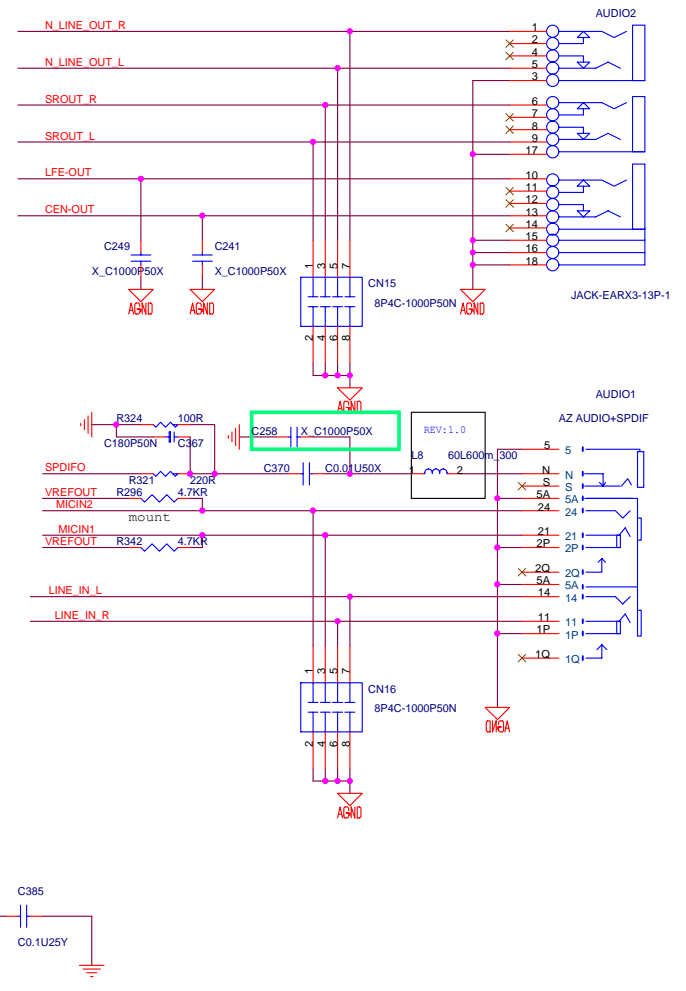
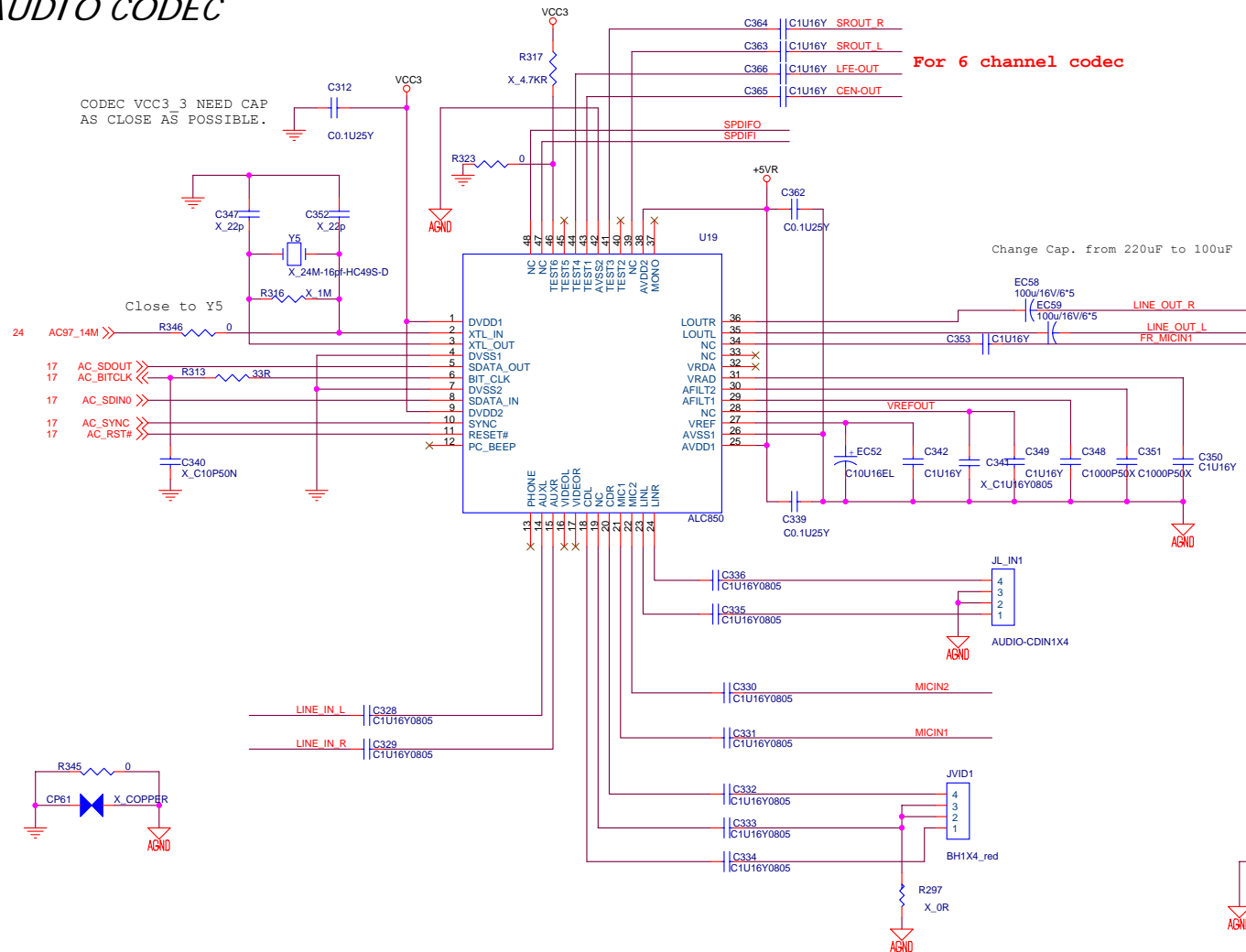
MICRO-STAR

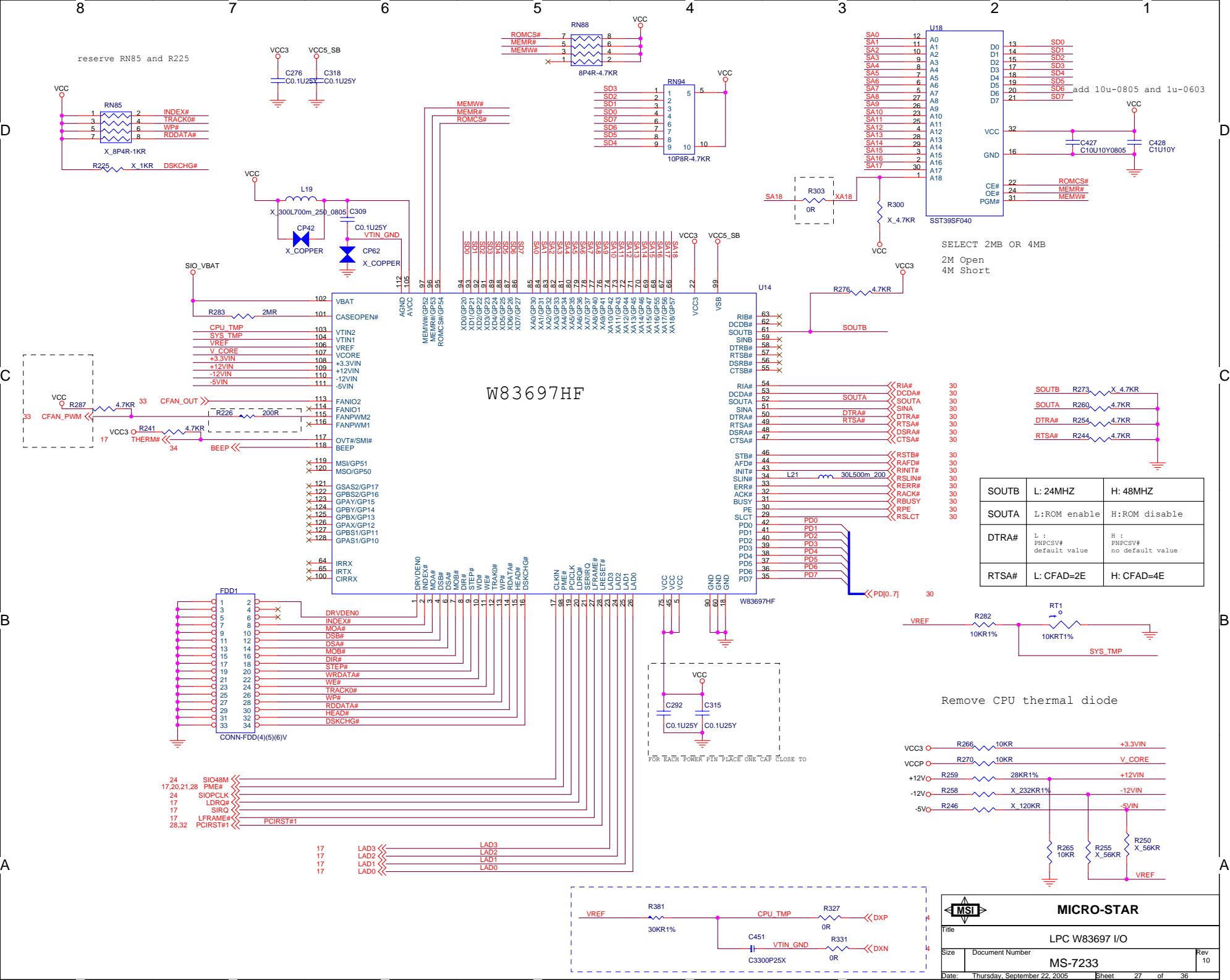
Title	Clock Buffer
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Size	Document Number
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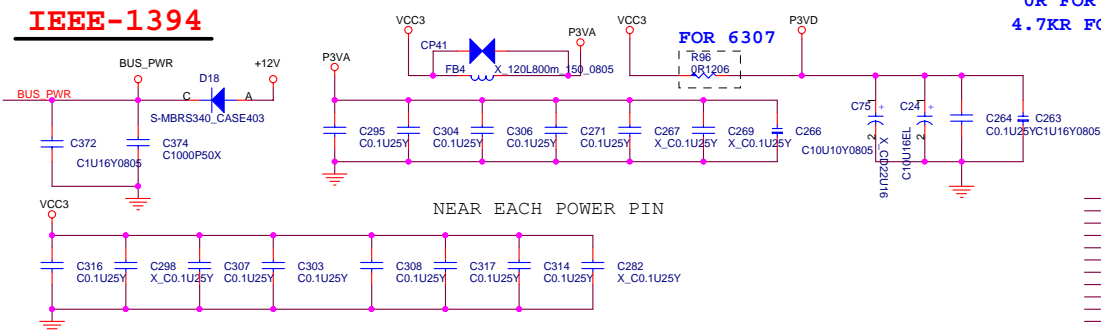
Rev	10
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AUDIO CODEC

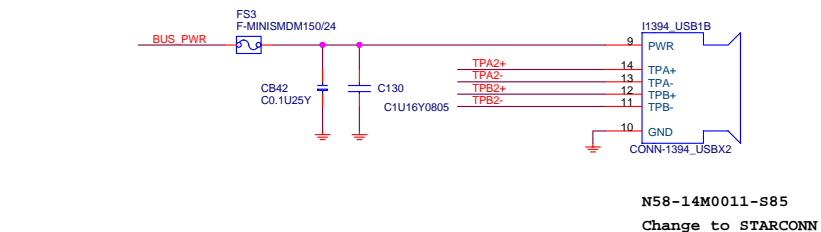
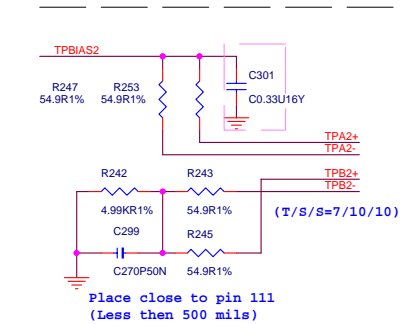
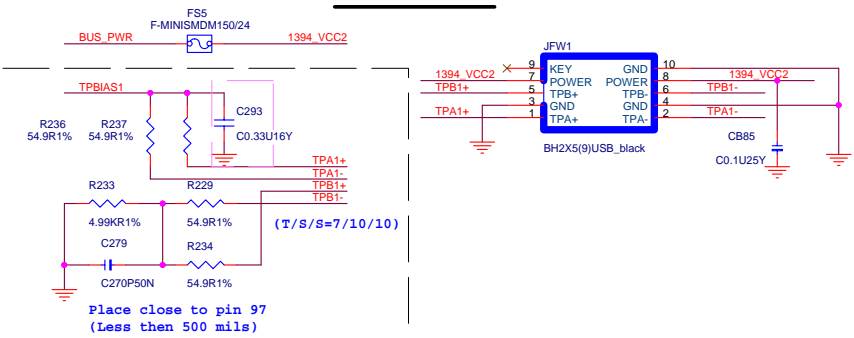




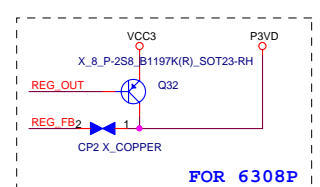
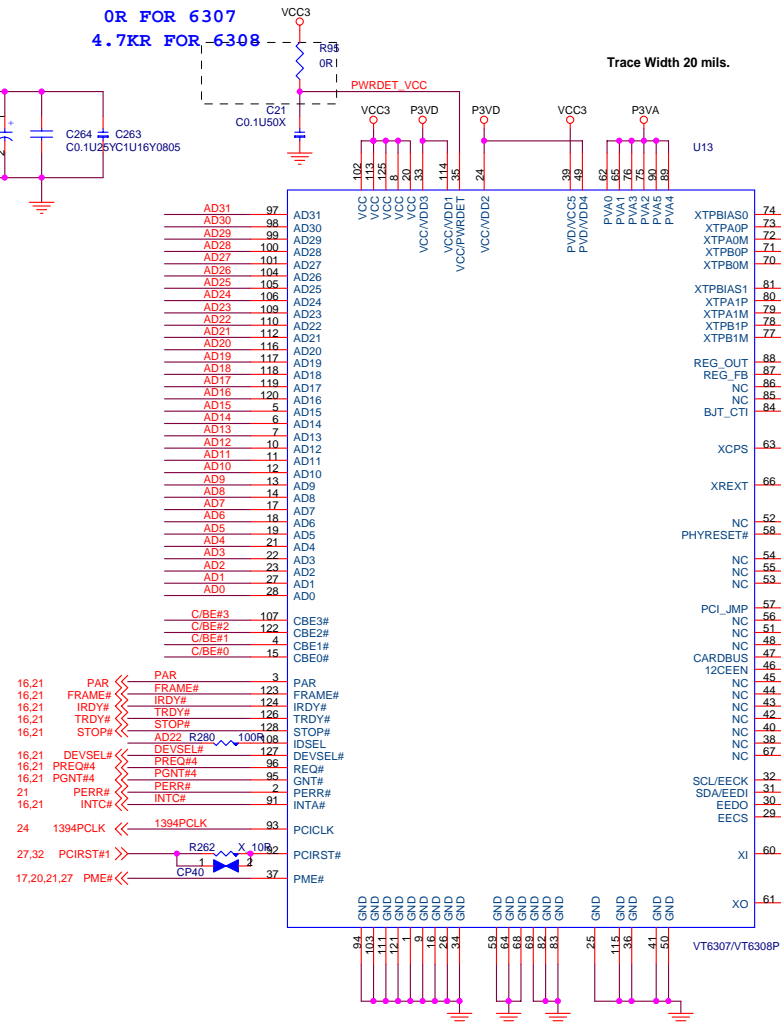
IEEE-1394



FRONT 1394 PORT 1

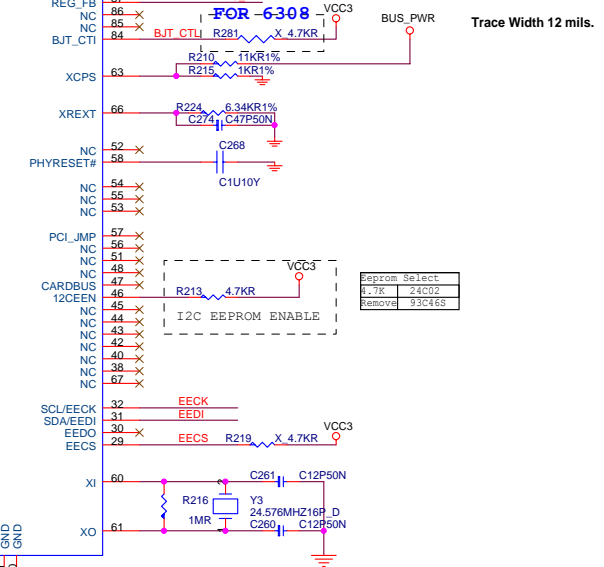


OR FOR 6307 4.7K FOR 6308



BJT_CTL

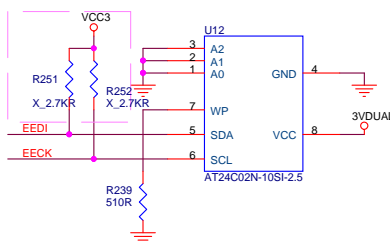
0: Internal power MOS
1: External BJT



IDSEL AD22 MASTER = PREQ#4 INTD#

16.21 AD[0..31] << AD[0..31]
16.21 C/BE#[3..0] << C/BE#[3..0]

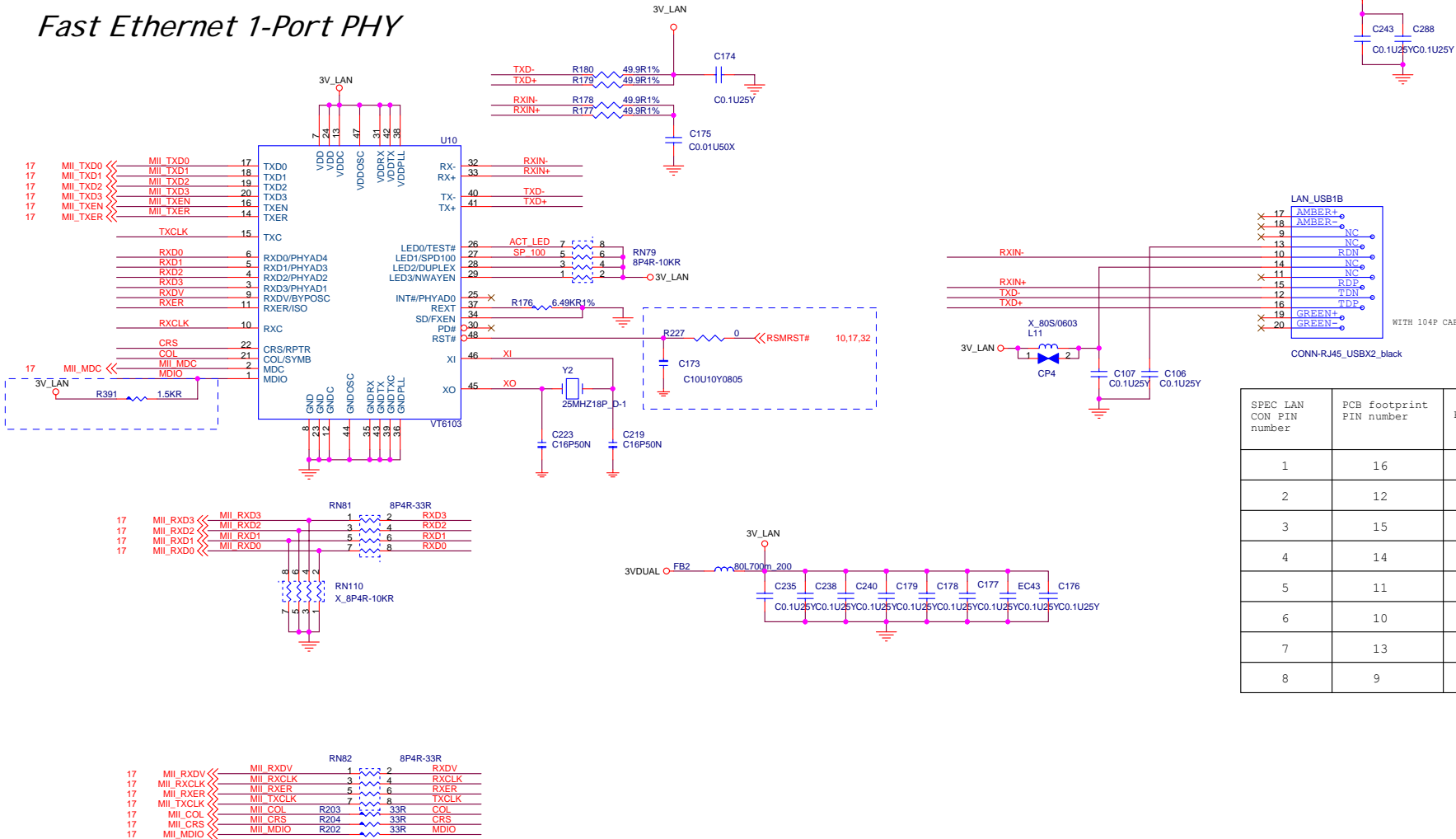
1394-EEPROM 24C02



MICRO-STAR

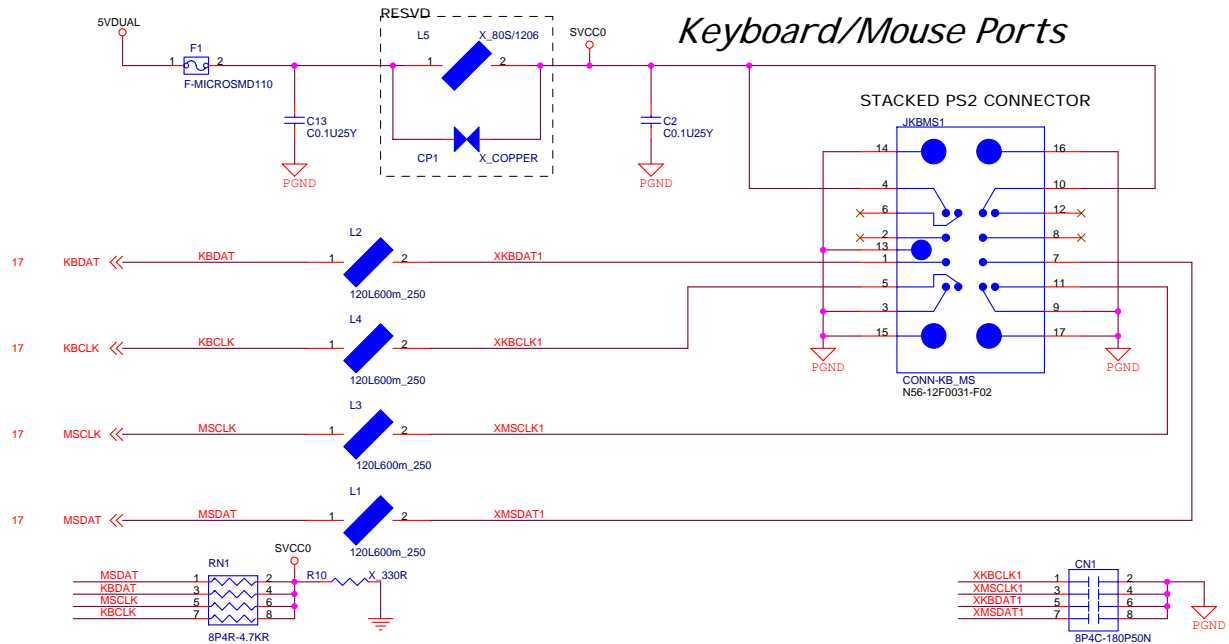
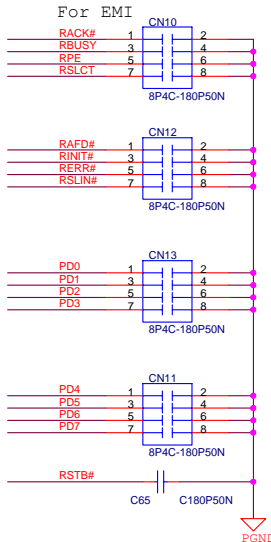
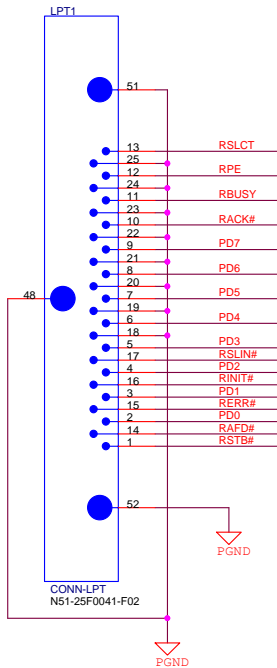
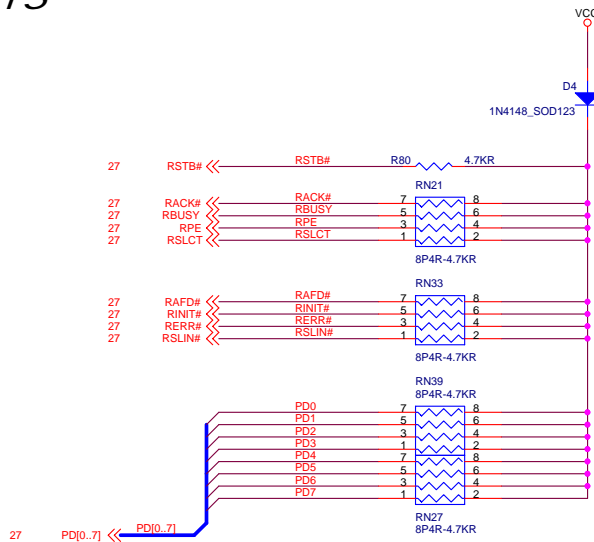
Title	1394 - VIA VT-6307	Rev	10
Size	Document Number	MS-7233	
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Fast Ethernet 1-Port PHY

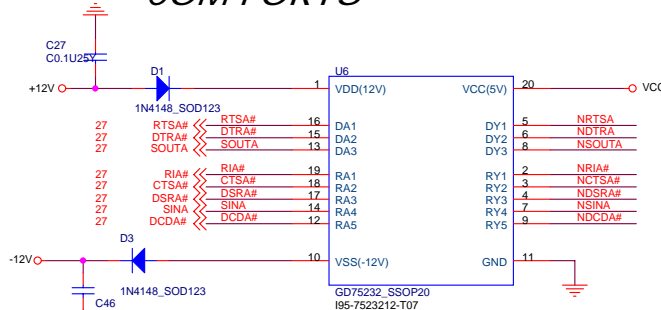


SPEC LAN CON PIN number	PCB footprint PIN number	PIN Define
1	16	TXD+
2	12	TXD-
3	15	RXIN+
4	14	TCT
5	11	NC
6	10	RXIN-
7	13	RCT
8	9	NC

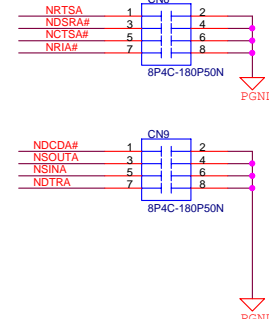
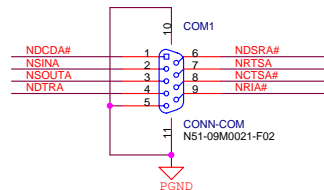
LPT PORTS



COM PORTS



Multiple RS232 Drivers and Receivers



MICRO-STAR

Title	LPT/COM PORT
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Size	Document Number
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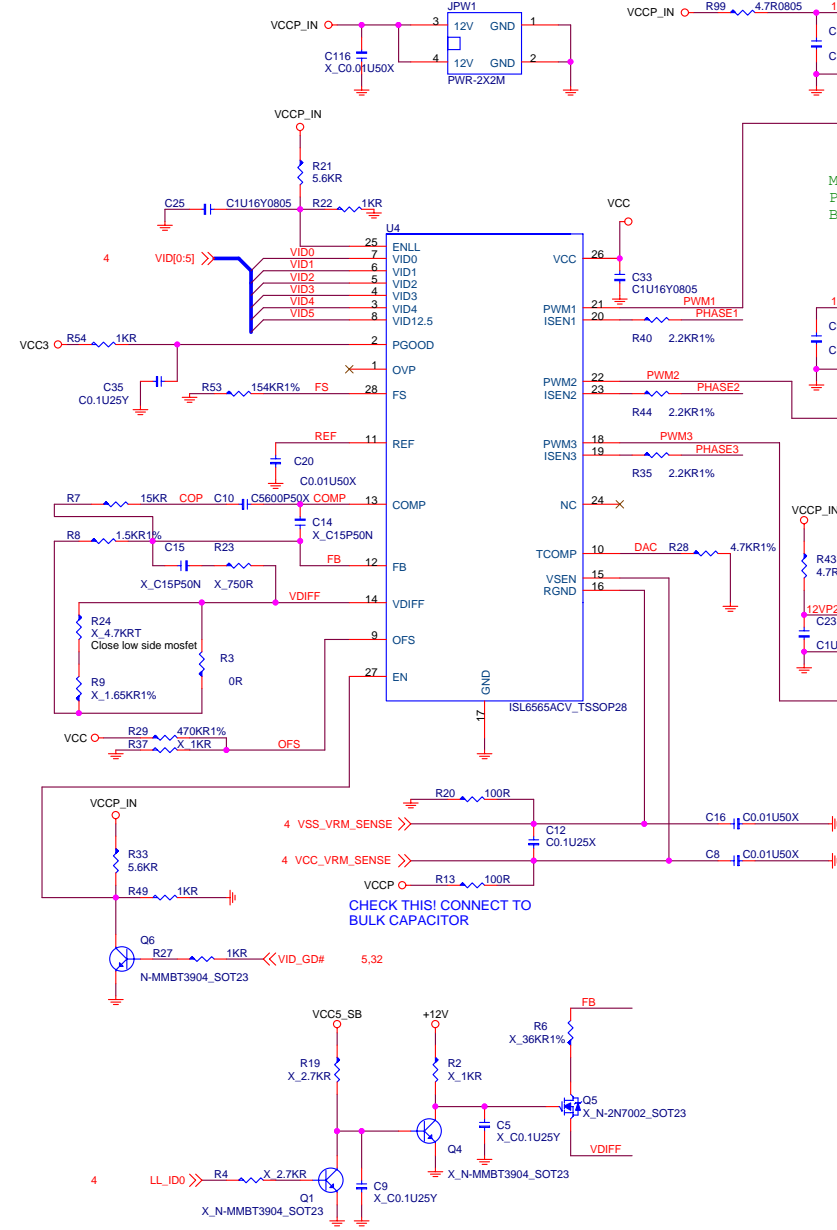
MS-7233

Rev
10

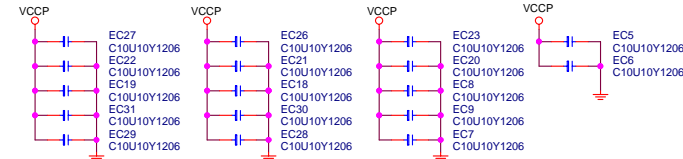
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	1
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Voltage Regular Module



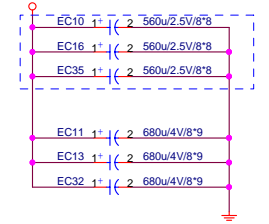
CPU DECOUPLING CAPACITORS



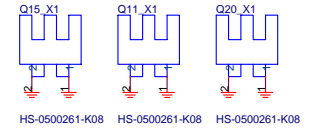
C10U10Y1206 10u/10V/Y5V, 1206, 80/-20%

Place these caps within socket cavity

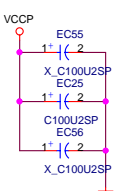
OS-CON Capacitors



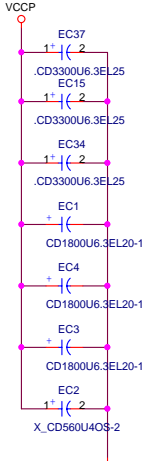
MOSFET Heatsinks



SP Capacitors



EL Capacitors



Solder Side



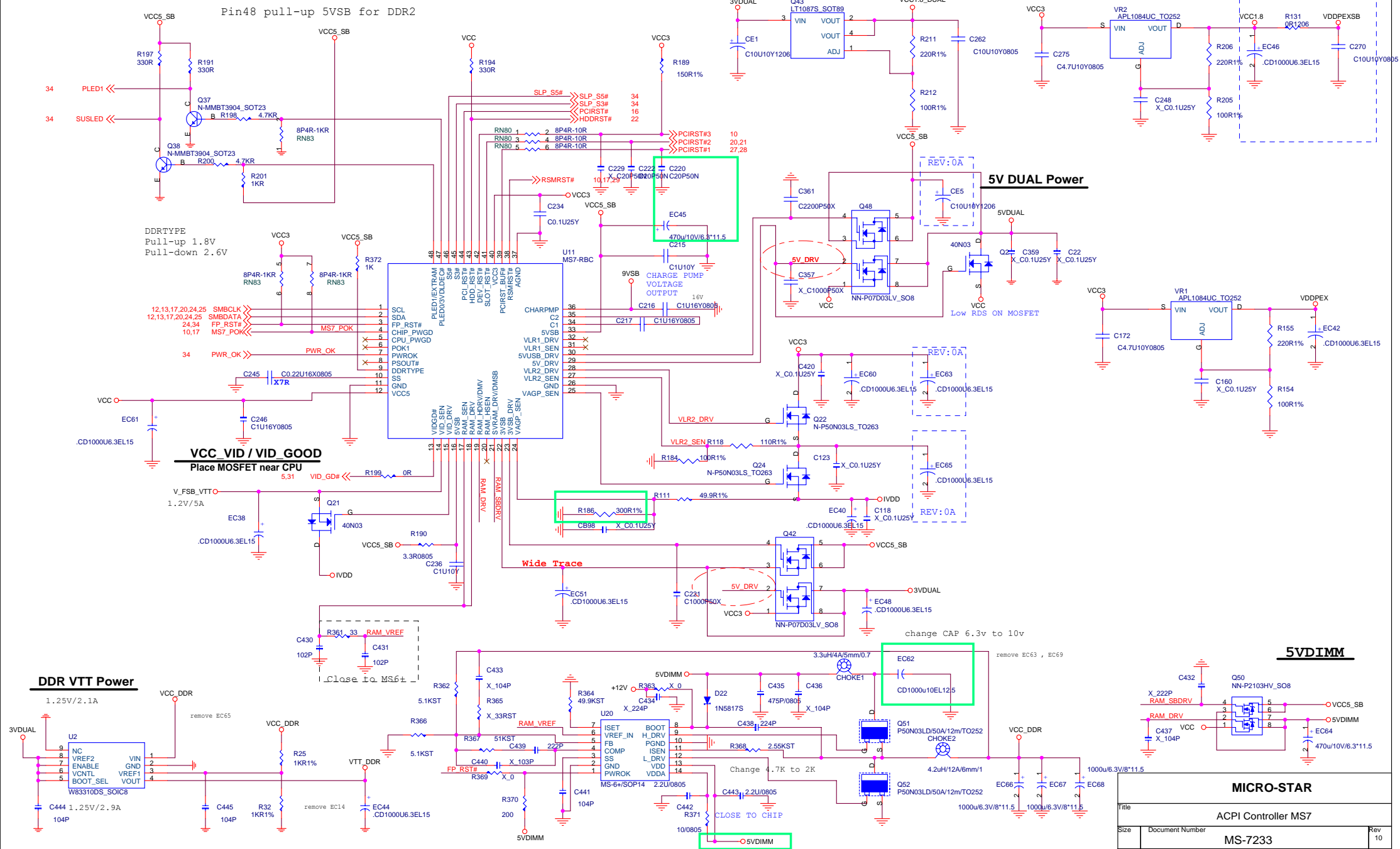
MSI MICRO-STAR			
Title VRM 10.1 - Intersil 6565ACV 3 Phase			
Size	Document Number	MS-7233	
Date	Thursday, September 22, 2005	Sheet	31 of 36

ACPI Controller

ICH5 300mA
PCI 375+20+20= 415mA

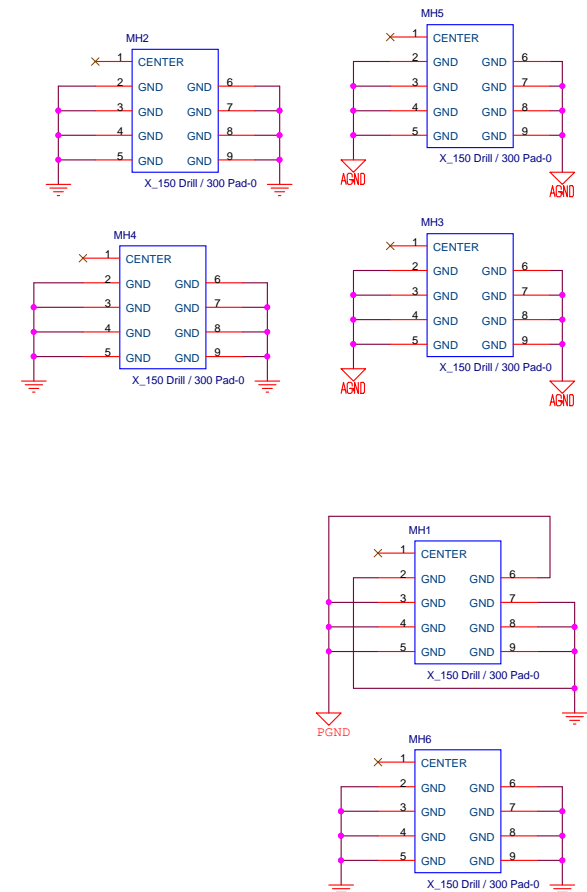
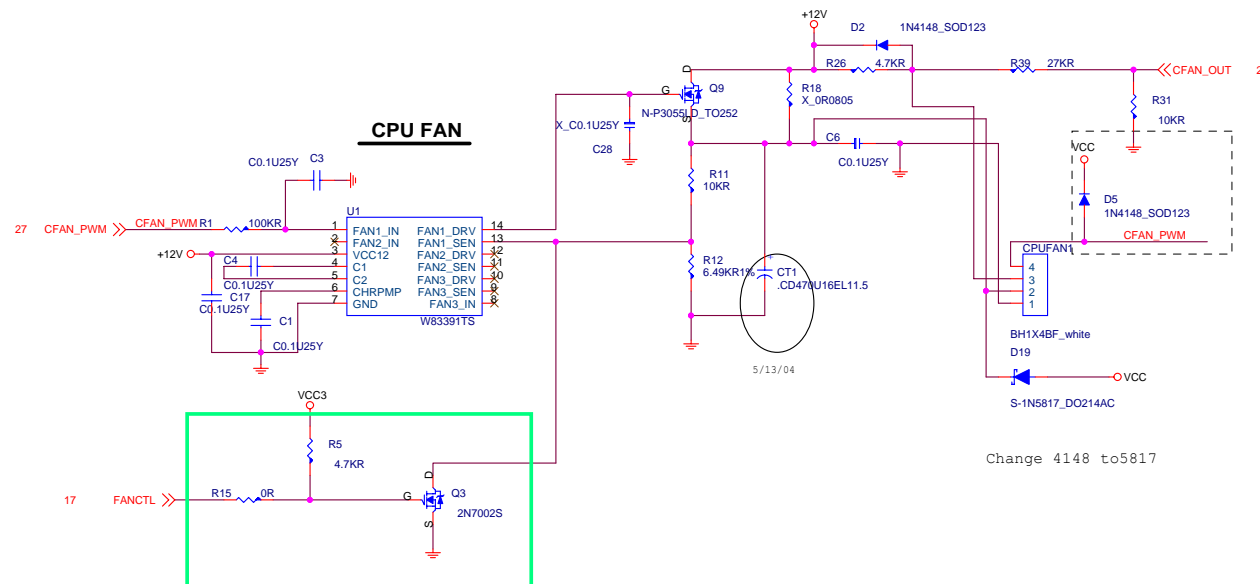
VCC3_SB 715mA

Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
MEM_STR	Main	Standby	0V

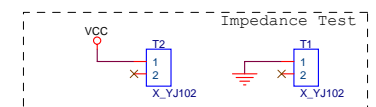
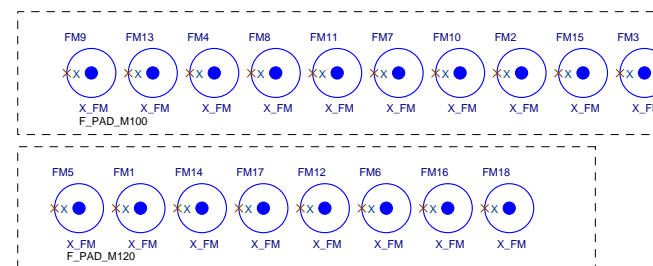
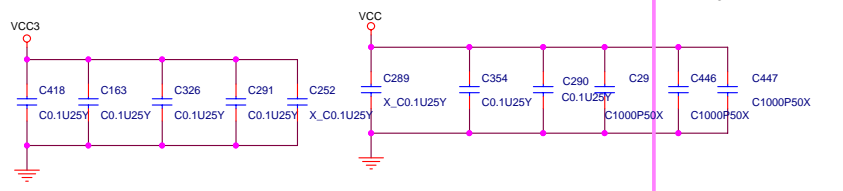


MICRO-STAR			
Title ACPI Controller MS7			
Size	Document Number	Rev	
	MS-7233	10	
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ATX VIA-Hole * 9

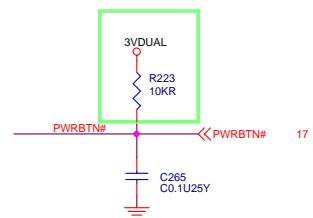
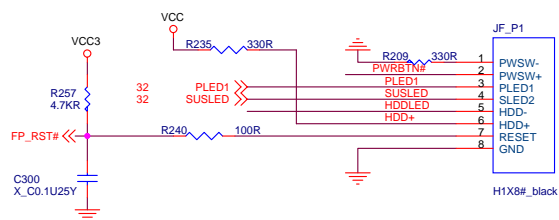


BULK / Decopuling

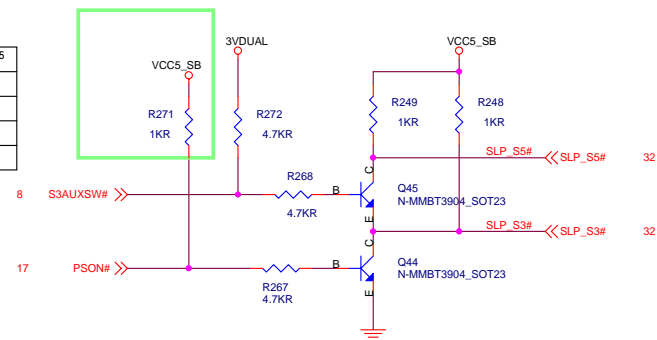


FRONT PANEL

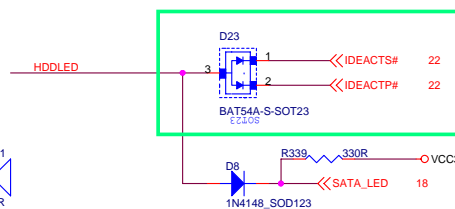
For MSI / Front Panel



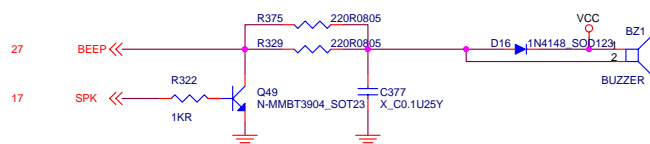
	S0	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S5#	1	1	0
SLP_S3#	1	0	0



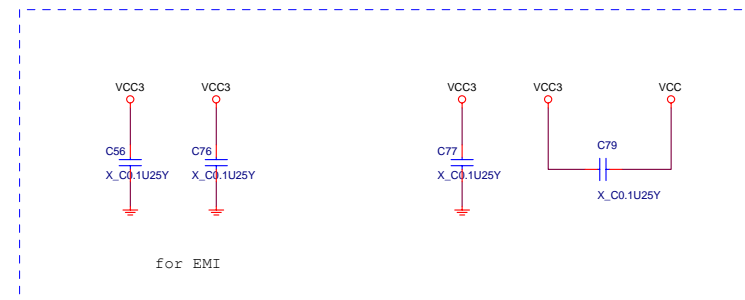
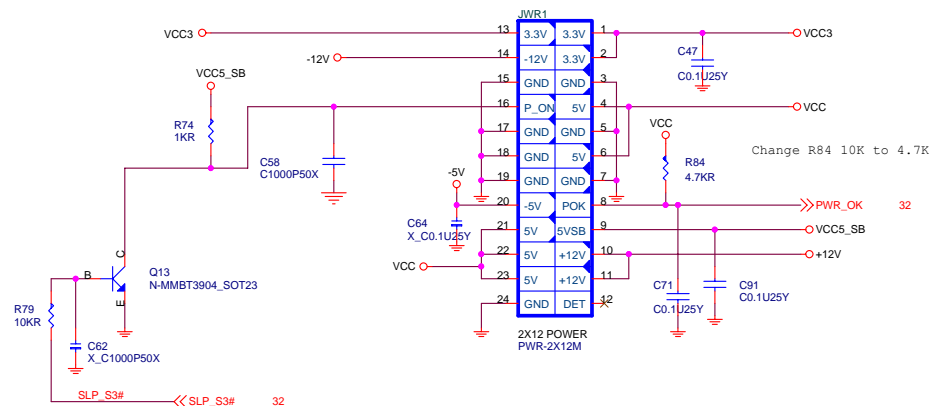
Change 8148*2 to BAT54A



Add 220R 0805



ATX Connector



MICRO-STAR

Title				FRONT PANEL			
Size	Document Number						Rev
	MS-7233						10
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